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Outstanding Surface Passivation for Highly Efficient Silicon Solar Cells Enabled by Innovative Al_yTiO_x/TiO_x Electron-Selective Contact Stack

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Passivating contacts based on transition metal oxides (TMOs) have the potential to overcome existing performance limitations in high-efficiency crystalline silicon (c-Si) solar cells, which is a significant driver for continuing cost/Watt reductions of photovoltaic electricity. Herein, innovative stacks of Al-alloyed TiO_x (Al_yTiO_x) and pure TiO_x as transparent electron-selective passivating contacts for n-type c-Si surfaces are explored. An optimized stack of 2 nm Al_yTiO_x and 2 nm TiO_x is shown to provide both record-quality surface passivation and excellent electrical contact, with a surface recombination current density prefactor J_0 of 2.4 fA cm^{-2} and a specific contact resistivity ρ_c of 15.2 mΩ cm^2. The performance of this innovative stack significantly exceeds previously reported values for pure or doped TiO_x single layers, SiO_x/TiO_x stacks, a-Si:H/TiO_x stacks, and other transparent contact technologies. Furthermore, an excellent efficiency of 21.9% is attained by incorporating the optimized stack as a full-area rear contact in an n-type c-Si solar cell. The findings set a new benchmark for the passivation performance of metal oxide-based passivating contacts, bringing it to a level on par with state-of-the-art SiO_x/poly-Si contacts while greatly improving optical transparency.

1. Introduction

To approach the theoretical efficiency limit of c-Si solar cells (≈29.43%),[1] carrier-selective passivating contacts exhibiting low recombination losses (low surface recombination current density, J_0), small resistive losses (low contact resistivity, ρ_c), and high transparency (no parasitic absorption) are essential. In conventional passivated emitter and rear cell (PERC) designs,[2] the direct contact between the metal contacts and the Si substrate results in significant recombination losses of photogenerated electrons and holes. While the use of heavily doped regions underneath the contacts significantly reduces contact recombination, it also results in increased Auger recombination and free carrier absorption, both of which limit the device's performance.[3] The losses associated with such contacts can be largely eliminated through the use of passivating carrier-selective contacts, which shield minority carriers from the contact metal while minimizing recombination at the Si surface. Excellent surface passivation combined with low contact resistivity has been demonstrated by carrier-selective contacts based on either doped hydrogenated amorphous silicon (a-Si:H) or polycrystalline Si (poly-Si), validated by record efficiencies in Si solar cells incorporating such contacts.[4] However, the limited optical transparency of a-Si:H or poly-Si results in significant parasitic absorption,[5] which limits performance when these contacts are applied to the illuminated side of a cell. Therefore, there is significant interest in developing new carrier-selective passivating contact technologies with similar electrical performance to Si-based

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/solr.202200550.

DOI: 10.1002/solr.202200550

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contacts but improved transparency. Transition metal oxides (TMOs) are leading candidates for this role as they are inexpensive, nontoxic, and abundant, can have substantial bandgap energies ($E_g > 3$ eV), a broad range of work functions (WFs) (from 3 to 7 eV), and conductivities ranging from insulating to metallic. This makes them very versatile when utilized as electron- or hole-selective heterocontacts.[6] Furthermore, these films can be deposited at low temperatures ($T \leq 200$ °C), implying a strong opportunity for process simplification and cost reduction.

The most promising results for TMOs as electron-selective passivating contacts (ESPCs) in c-Si solar cells have been demonstrated by amorphous TiO_2 thin films prepared by the atomic layer deposition (ALD) technique.[3,6,7] Amorphous TiO_2 is a promising candidate for insertion between the c-Si/metal interface as it has a sufficiently low WF with a small conduction band offset (CBO) and a large valence band offset (VBO) with c-Si, in addition to providing good level of surface passivation. For example, a 4.5 nm SiO_x/TiO_2 stack was reported to provide a surface recombination velocity (S_{eff}) of 17 cm s^{-1} together with contact resistivity of 47 mΩ cm^2 on n-type c-Si.[8] Furthermore, a remarkable efficiency of 22.1% has been achieved for an n-type c-Si solar cell featuring a full-area SiO_x/TiO_2 rear contact.[9] However, the efficiency of the best TiO_2-based devices is still significantly lower than that of cells based on poly-Si passivating contacts. This is due to a number of factors, including the reduced surface passivation provided by very thin films (less than 5 nm) of TiO_2,[10] the deterioration of surface passivation following metallization due to probable TiO_x–metal interaction,[11] and thermal stability issues for these ultrathin layers.[8,9,10b]

In order to overcome these limitations, one approach is to introduce an interlayer of another material or to "dope" the TiO_2 layer with other elements. Al_2O_3 is a common choice as interlayer or dopant species due to the ready availability of TMA as an Al precursor and the excellent characteristics of the TMA + H_2O ALD process, as well as the well-known outstanding properties of Al_2O_3 as a passivation layer for c-Si surfaces.[12] Liang et al. found that doping small concentrations of Al in TiO_2 helped to suppress crystallization and the resulting loss of passivation that normally occurs in thicker layers following annealing.[13] The resulting 15 nm Al-doped TiO_2 demonstrated good thermal stability with a reasonably low surface recombination current density prefactor J_0 of 100 fA cm^{-2} after annealing at 350 °C; however, this thickness is likely too thick to act as an effective contact. In a separate work, Liu et al. varied the Al:Ti cycle ratio to form Al-doped TiO_2 films, obtaining an effective minority carrier lifetime τ_{eff} of 1.9 ms and contact resistivity ρ_c of 100 mΩ cm^2 on Si using an optimized $Al_{0.20}Ti_{0.36}O$ layer with LiF/Al contacts, after annealing at 300 °C.[14] Although doping with aluminum was found to improve surface passivation quality and reduce contact resistivity in this case, the obtained contact resistivity was still relatively high (100 mΩ cm^2). In addition, we believe that the use of the transmission line measurement (TLM) method to measure contact resistivity makes the obtained contact resistivity values unreliable due to the high film thickness (16.5 nm). This optimized film was applied as a passivation layer to the illuminated side of p-type PERC solar cells, resulting in 21.43% efficiency, compared with 21.13% for a cell with undoped TiO_x (it should be noted however that in this case the contacts were formed using a fire-through paste, so it is not clear that the film provided any contact passivation). Note that in these previous works, Al was conceived of essentially as a dopant element, and therefore applied at low concentrations (Al/(Al+Ti) < 0.35), in contrast to the present work, where Al is alloyed with TiO_x at much higher concentrations (even as the majority constituent). At such concentrations, Al can be expected not merely to modulate the properties of the TiO_x film (e.g., by increasing the carrier concentration or impeding crystallization), but actually to form a distinct hybrid material with properties intermediate between the constituents.

In addition, several authors have investigated contact structures based on the use of Al_2O_3/TiO_2 stacks; however, in most cases the presence of the Al_2O_3 layer results in unacceptably high contact resistivities.[15] The best result with such a structure appears to be that of Masmitjà et al., who obtained a contact resistivity of 2.5 mΩ cm^2 and surface recombination velocities below 40 cm s^{-1} ($J_0 = 140$ fA cm^{-2}) for an Al_2O_3 (6 ALD cycles)/TiO_2 (20 ALD cycles)/Mg stack.[16] This stack was applied in an interdigitated back-contacted (IBC) Si solar cell structure, yielding 19.1% efficiency.[16] Other authors studied thick (noncontacting) Al_2O_3/TiO_2 stacks as dielectric passivation/antireflection coating layers and demonstrated a high level of silicon surface passivation as well.[17] We note a recently published review article that gives a detailed discussion of Al_2O_3/TiO_2-based layers and their application to the passivation of Si surfaces.[18]

A general trend apparent in these previous studies is that improving the surface passivation of pure or doped TiO_2 single layers or Al_2O_3/TiO_2 stacks generally comes at the expense of increasing contact resistivity and vice versa. In this work, we demonstrate an innovative method for obtaining outstanding silicon surface passivation combined with low contact resistivity using a combination of Al-alloyed TiO_x (Al_yTiO_x) and pure TiO_x to form an innovative Al_yTiO_x/TiO_x stack. Film thickness, deposition temperature, and the order of deposited layers are varied systematically to optimize J_0 and contact resistivity. In addition, spectroscopic ellipsometry, grazing-incidence X-ray diffraction (GIXRD), X-ray photoelectron spectroscopy (XPS), and ultraviolet photoelectron spectroscopy (UPS) are applied to characterize the thickness, optical properties, crystallinity, composition, and energetic properties of the deposited layers. Finally, the optimized layer is integrated into proof-of-concept laboratory solar cells to demonstrate its performance at a device level.

2. Results and Discussion

Prior to presenting the results for contact resistivity, surface passivation, and device performance, it is worth noting that the material properties of the TiO_x and Al_yTiO_x films were characterized comprehensively using the following techniques: spectroscopic ellipsometry, GIXRD, UPS, XPS, and energy-dispersive X-ray spectroscopy (EDS). A detailed presentation and discussion of these results is given in the Supporting Information (Figure S2–S7). The resulting details of the structure, refractive indices (n), bandgap energies (E_g), WFs, valence band maxima (VBM), conduction band minima (CBM), VBO,

Table 1. Material properties of TiO_x and Al_yTiO_x layers deposited at 75 °C. n is the refractive index and E_g is the optical bandgap. WF, VBM and CBM energies are given relative to the vacuum level.

Film	Structure	Optical properties		UPS analysis [eV]					XPS analysis [at%]			
		n at 632.8 nm	E_g [eV]	WF	VBM	CBM	VBO	CBO	Ti	Al	Cl	O
TiO_x	amorphous	2.24	3.37	4.12	7.32	3.95	2.15	0.1	24.9	–	6.3	68.8
Al_yTiO_x	amorphous	1.75	3.75	3.42	7.22	3.47	2.05	0.58	5.3	18.9	4.1	71.7

CBO, and elemental composition (Ti, Al, Cl, O) for the TiO_x and Al_yTiO_x layers are also summarized in **Table 1**.

2.1. Contact Resistivity

The choice of a contact metal with an appropriate WF is critically important to the effective operation of metal–oxide carrier-selective contacts. Based on current–voltage measurements of metal/Si and metal/TMO/Si structures, explained in detail in the Supporting Information (Figure S8), calcium (Ca) was selected as the top-contact metal and a thick layer of Al as a capping layer for contact resistivity measurements. **Figure 1**a–d shows schematic diagrams of the samples used to determine the specific contact resistivity ρ_c via the Cox–Strack method.[19] Single films of TiO_x and Al_yTiO_x, as well as TiO_x/Al_yTiO_x and Al_yTiO_x/TiO_x stacks, were investigated. All films and stacks were deposited at 75 °C. A heavily doped n^{++} region on the rear side was used to minimize the resistance contribution of the rear contact. The dark current–voltage (I–V) measurements for these samples are shown in Figure S9a–d (Supporting Information). All structures exhibited Ohmic I–V behavior in the investigated thickness range (2, 2.5, 3, 3.5, 4 nm) except for the Al_yTiO_x single layers with thickness > 2.5 nm, which showed weak rectification behavior as illustrated in Figure S9b (Supporting Information). From UPS analysis and the bandgap energy of Al_yTiO_x, the CBO between Al_yTiO_x and c-Si was calculated to be 0.58 eV, which is large enough to present a barrier to electron transport for thicker Al_yTiO_x films, beyond the thickness where tunneling transport is dominant. Additionally, the XPS measurement of the Al_yTiO_x film reveals that the concentration Al in the film is significantly higher than Ti, indicating that the Al_yTiO_x film could possess insulating behavior. All of these factors likely contribute to the rectifying behavior of the thicker Al_yTiO_x films.

The combination of Al_yTiO_x with pure TiO_x in a stack has the advantage that it reduces the thickness of the Al_yTiO_x layer for a given total stack thickness, resulting in Ohmic contact even for thicker stacks up to 4 nm, with a corresponding reduction in extracted ρ_c. Figure 1e shows a comparison of the thickness dependence of ρ_c for the four investigated structures (shown in Figure 1a–d). The TiO_x films exhibited the lowest contact resistivity of the examined structures, which is consistent with the lower value of $CBO_{TiOx} = 0.1$ eV, while no significant difference in contact resistivity was exhibited by the stacks based on the stacking order of the TiO_x and Al_yTiO_x layers. As shown in Figure 1e, a weak thickness dependence of ρ_c is apparent for the TiO_x single layers and stacks.

In order to help understand the electron selectivity of the investigated heterocontacts, the corresponding energy-level diagrams are shown in Figure 1a–d In this specific case, the electron selectivity is achieved through the use of two strategies: 1) by forming a heterojunction between n-Si and wide-bandgap TMO materials with small CBOs, $CBO_{TiOx} = 0.1$ eV and $CBO_{AlyTiOx} = 0.58$ eV (which would enable electron transport

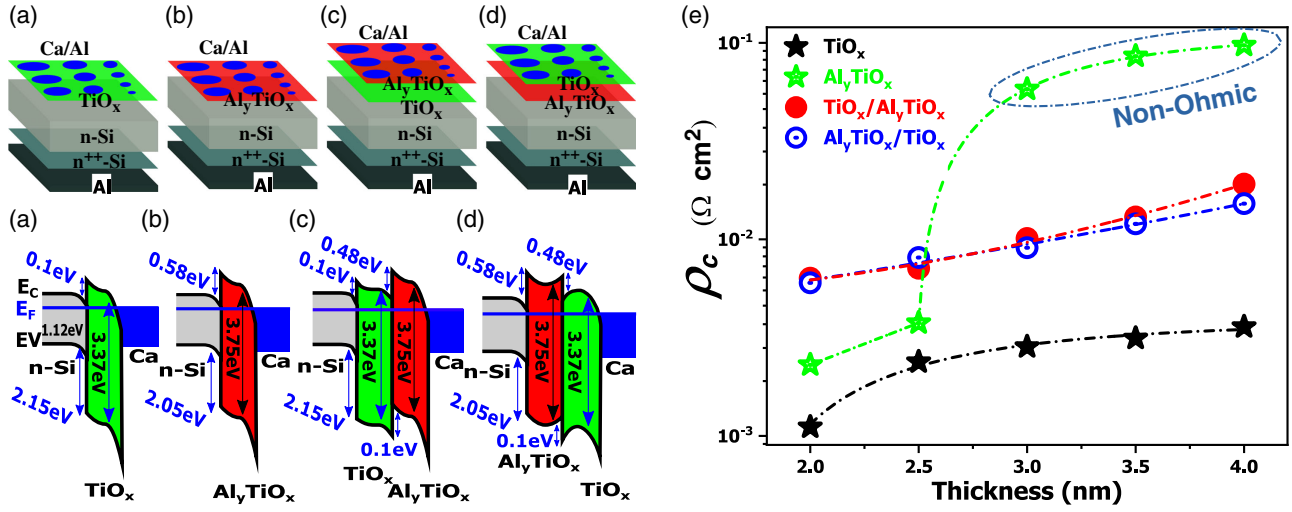

Figure 1. Schematic diagrams of sample structure used for contact resistivity measurements by the Cox–Strack method and the corresponding schematic energy-level diagrams for a) pure TiO_x, b) Al_yTiO_x, c) TiO_x/Al_yTiO_x stacks, and Al_yTiO_x/TiO_x stacks. All films were deposited at 75 °C on planar silicon substrates (1 Ω cm, 165 µm). e) Contact resistivity of Al/Ca/TiO_x/n-Si, Al/Ca/Al_yTiO_x/n-Si, Al/Ca/TiO_x/Al_yTiO_x/n-Si, and Al/Ca/Al_yTiO_x/TiO_x/n-Si structures, as a function of the total oxide film or stack thickness. In the stack structures, the total thickness is divided equally between TiO_x and Al_yTiO_x layers.

from n-Si to TMO), and large VBOs, $VBO_{TiOx} = 2.15$ and $VBO_{AlyTiOx} = 2.05$ eV (which would block hole transport from n-Si to TMO) and 2) the use of an external potential source, which in our work is a combination of a low-work-function metal ($\varphi_{Ca} = 2.9$ eV) and low-work-function TMOs ($\varphi_{TiOx} = 4.12$ eV, $\varphi_{AlyTiOx} = 3.42$ eV). The aforementioned factors will combine to induce strong downward band bending at the *n*-Si/TMO interfaces, resulting in a decrease in the surface concentration of minority charge carriers (holes) and an increase in the concentration of majority charge carriers (electrons), all of which result in a decrease in surface recombination.

2.2. Surface Passivation

Before presenting the surface passivation results of these heterocontact structures, we would like to make clear a point that is perhaps not widely recognized or made clear in earlier literature, which is that thin films of pure ALD TiO_2 from $TiCl_4 + H_2O$ can efficiently passivate double-side-polished (100) Si surfaces, but apparently not planar (100) surfaces prepared by chemical etching, particularly when the TiO_2 thickness is less than 5 nm. This observation is consistent with a previous study, where the surface recombination current density prefactor (J_0) was found to increase strongly for thinner films of TiO_2 on n-type FZ (100) c-Si substrates etched in TMAH.[10a] The latter chemically etched planar surfaces are more relevant for commercial Si solar cells and were used in this work to develop the novel stack, which as we shall show has demonstrated significant success in passivating them. Using these planar Cz (100) n-type c-Si substrates, numerous stacks were explored to discover the optimal stack configuration (based on the lowest extracted value of J_0) as shown in Figure S10 (Supporting Information). The surface passivation performance of the optimized stack (Al_yTiO_x/TiO_x) was then compared with that of TiO_x, Al_yTiO_x single layers, and a mirrored stack structure (TiO_x/Al_yTiO_x), as discussed in the next section.

Figure 2a–d shows schematic diagrams of the symmetrical sample structures used for surface passivation studies. The implied open-circuit voltage (iV_{oc}) is widely used to quantify the quality of c-Si surface passivation, especially for passivating contacts, since it can be directly related to the potential device performance. Figure 2e shows the dependence of iV_{oc} on thickness for TiO_x and Al_yTiO_x single layers, as well as TiO_x/Al_yTiO_x and Al_yTiO_x/TiO_x stacks, deposited at 75 °C on planar (100) n-type c-Si substrates with thickness of ≈105 µm (≈7–10 Ω cm). We observed that undoped TiO_x offered the worst surface

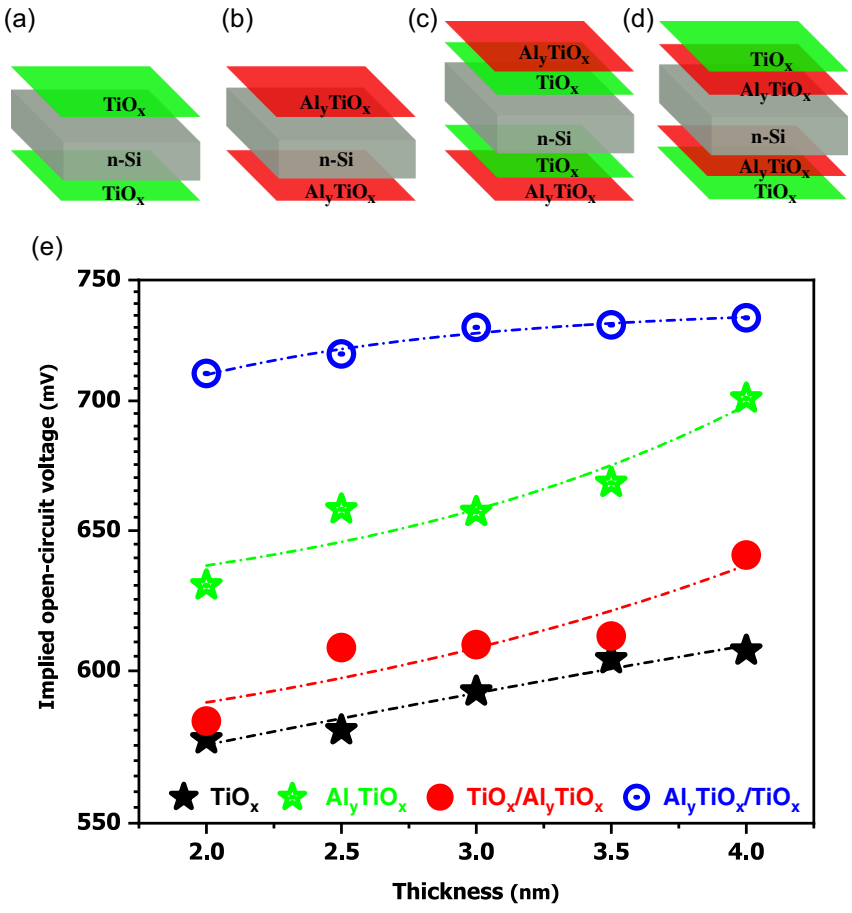

Figure 2. Schematic diagrams of symmetrical sample structures used for lifetime measurements of a) TiO_x, b) Al_yTiO_x, c) TiO_x/Al_yTiO_x stacks, and d) Al_yTiO_x/TiO_x stacks. All films were deposited at 75 °C on planar silicon substrates (7–10 Ω cm, 105 µm). e) Implied open-circuit voltage of lifetime samples passivated by pure TiO_x, Al_yTiO_x, TiO_x/Al_yTiO_x stacks, and Al_yTiO_x/TiO_x stacks, as a function of the total film or stack thickness.

passivation for these surfaces and that single Al_yTiO_x layers provided better passivation than a TiO_x/Al_yTiO_x stack. Although pure TiO_x provided the worst passivation ($iV_{oc} = 607$ mV for 4 nm), it also provided the lowest contact resistivity.

Surprisingly, significantly improved surface passivation was obtained simply by switching the order of the TiO_x and Al_yTiO_x layers to construct the Al_yTiO_x/TiO_x stack shown in Figure 2d. This contrasts with the apparent independence of contact resistivity on stacking order. The injection level-dependent effective minority carrier lifetime (τ_{eff}) of n-Si substrates passivated by the novel Al_yTiO_x/TiO_x stack with varying total thickness is represented in Figure S11a (Supporting Information), while the corresponding iV_{oc}, τ_{eff}, and J_0 are summarized in Figure S11b (Supporting Information). The minority carrier lifetime at an injection level of 10^{15} cm^{-3} improves from 828 µs to 3.9 ms as the total stack thickness increases from 2 nm to 4 nm. At the same time, the iV_{oc} improves from 711 to 733 mV, while J_0 reduces from 5.7 to 2.4 fA cm^{-2} with increasing stack thickness. It is worth noting that the value obtained for the surface recombination current density prefactor ($J_0 < 3$ fA cm^{-2} for 4 nm) of our Al_yTiO_x/TiO_x stack is significantly better than that reported in prior works for doped or pure TiO_2 surface passivation of c-Si, particularly for the studied thickness range (2–4 nm).

Passivating contacts for high-efficiency c-Si solar cells should exhibit low recombination losses (excellent surface passivation) combined with low resistive losses (low contact resistivity). To demonstrate that our optimized stack affords superior surface passivation while maintaining low contact resistivity, **Figure 3**a plots the variation in contact resistivity as a function of implied open-circuit voltage (iV_{oc}) for the examined structures of varied thickness. It is clear from this plot that the optimized stack offers excellent surface passivation in conjunction with a low specific contact resistivity compared with the other structures studied. Indeed, the values obtained for the optimized stack are truly exceptional, as shown in Figure 3b, where we compare it to previously reported ESPCs, including TiO_x,[8,20] SiO_x/TiO_x,[8] a-Si:H/TiO_x,[21] TiO_xN_y,[10c] a:Si-H/TiO_xN,[10c] MgF,[22] a:Si-H/MgF,[22] SiO_x/ITO,[7a] SiO_x/Nb_2O_5,[23] MgO,[24] TaN,[25] Al_2O_3/TiO_x,[16] a-Si:H/n-a-Si:H,[7a] and SiO_x/n^+-poly-Si,[7a,26] in terms of J_0 and ρ_c. This figure shows that the investigated stack (Al_yTiO_x/TiO_x) significantly outperforms previously reported metal oxide-based contacts. Indeed, its performance is closely comparable with state-of-the-art SiO_x/n^+-poly-Si passivating contacts (which unlike it have poor transparency). Therefore, it can be concluded that we have succeeded in discovering a novel method for obtaining ESPCs based on TiO_x that demonstrate superior performance to prior reported ESPC technologies.

2.3. Surface Passivation Mechanism

An interesting question is why the Al_yTiO_x/TiO_x stack exhibits better surface passivation compared with the other structures explored in this study or any previous reports on TiO_2/c-Si surface passivation. This question may be addressed by comparing our optimized stack to other stacks from the literature that are roughly comparable, in particular Al_2O_3/TiO_2 stacks. As noted in Introduction, such stacks were originally explored as dielectric passivation/antireflection stacks for c-Si solar cells. In particular, Suh et al. reported significant improvements in passivation following deposition of TiO_2 at 200 °C (using $TiCl_4$ and H_2O as in our study) on Al_2O_3-passivated samples previously annealed at 400 °C in forming gas. The improvement was traced primarily to a significant reduction of the interface trap density D_{it}, with a stack of 10 nm Al_2O_3/30 nm TiO_2 achieving an outstanding low D_{it} of 1.1×10^{10} cm^{-2} eV^{-1} at midgap, compared with

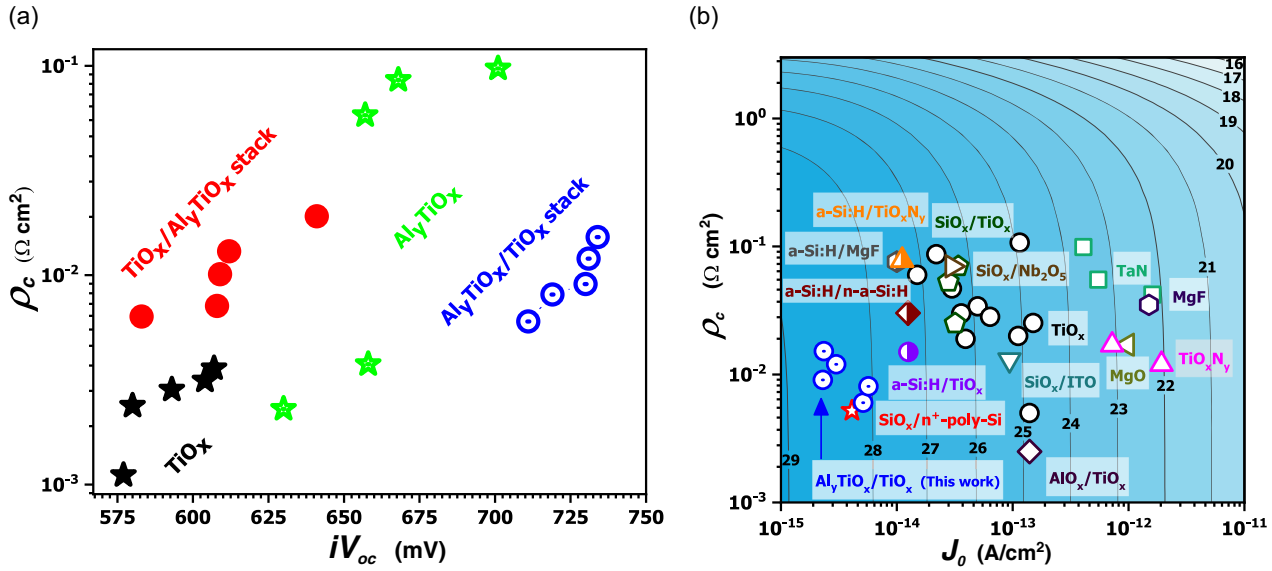

Figure 3. a) Contact resistivity versus implied open-circuit voltage for pure TiO_x, Al_yTiO_x, TiO_x/Al_yTiO_x stacks, and Al_yTiO_x/TiO_x stacks. All films were deposited at 75 °C on planar silicon substrates (7–10 Ω cm, 105 µm). b) Contact resistivity ρ_c versus surface recombination current density prefactor J_0 for our novel stack in comparison with other previously reported ESPCs (references given in the text). J_0 was calculated from reported lifetime or surface recombination velocity values.[26] Contours show the corresponding efficiency limit for a 100 µm-thick, undoped Si solar cell (with ideal Lambertian light trapping), assuming a full-area rear contact with these properties, as simulated using Quokka3.

$\approx 1 \times 10^{11}\,cm^{-2}\,eV^{-1}$ prior to TiO_2 deposition.[17d] The reduction of D_{it} was interpreted to possibly be the result of atomic H release on TiO_2 deposition, where this H might then diffuse through the TiO_2 and Al_2O_3 films and passivate Si dangling bonds.[17d] Besides this, Cl atoms are also known to be effective at passivating Si dangling bonds. For example, in the case of ALD Al_2O_3, the chlorine content provided by dimethylaluminum chloride (DMACl) appears to reduce interface trap density relative to that achieved with trimethylaluminum (TMA).[27] This might be because chlorine provides additional passivation of silicon dangling bonds by forming Si—Cl bonds.[27,28] Similarly, we expect a very-low-interface trap density in our samples based on the remarkable surface passivation ($J_0 < 3\,fA\,cm^{-2}$) achieved by the optimized Al_yTiO_x/TiO_x stack. Unfortunately, this prediction cannot be verified using capacitance–voltage measurements in our case due to the significant leakage current caused by the high conductivity of the stack. However, we speculate that the superior chemical surface passivation in our stack might result from passivation elements such as atomic H and Cl being freed during the deposition process and subsequently diffusing across the stack, passivating Si dangling bonds. We note that the concentrations of Cl in the Al_yTiO_x and TiO_x films deposited at 75 °C, according to our XPS analysis, are 4.1 and 6.3 at%, respectively. In addition, the concentration of atomic H in TiO_2 films similar to ours (deposited at 80 °C by ALD using $TiCl_4$ and H_2O) was reported to be ≈2.6 at%.[29] To put this into perspective, a hydrogen content of 2–3 at% in Al_2O_3 is sufficient to provide highly effective passivation of defects at the Si/SiO_x interface formed when Al_2O_3 is deposited to H-terminated Si surface.[30] It is worth mentioning that surface passivation layers commonly require an anneal at elevated temperatures to "activate" the passivation, whereas the stacks investigated in this work provide full passivation as deposited, without any annealing. This is consistent with the behavior previously observed for TiO_2 deposited from $TiCl_4$ and H_2O.[10a]

2.4. Influence of Stack Properties

In the following sections, we report the influence of the relative thickness of the layers in the stack, the total stack thickness, the order of the precursor subcycles, the composition of the non-TiO_x layer, and the effect of deposition temperature on the surface passivation quality of this novel stack. For these studies, double-side-polished 2.5 Ω cm n-type FZ (100) Si substrates with a thickness of ≈285 μm were used.

In an attempt to gain a better understanding of this remarkable surface passivation and to identify the relative contributions of the different layers in the stack, various types of stacks were deposited at 75 °C, as indicated in the inset of **Figure 4**a. These stacks were prepared by varying the thickness of each layer in the stack while maintaining the total thickness of the stack at 4 nm. The surface passivation performance of the five stacks is summarized in Figure 4b in terms of τ_{eff}, iV_{oc}, and J_0. It is observed to be significantly dependent on the thickness of each layer in the stacks. Interestingly, Stack #2, with an equal thickness of Al_yTiO_x and TiO_x, demonstrated the best passivation with $\tau_{eff} = 6.5$ ms, $iV_{oc} = 732$ mV, and $J_0 = 2.8\,fA\,cm^{-2}$. When the thickness of the Al-alloyed layer (Al_yTiO_x) was reduced to 1 nm (Stack #1), the resulting surface passivation obtained was close to that of Stack #2; however, when the thickness of the Al-alloyed layer was increased to 3 nm (Stack #3), the surface passivation obtained was the poorest among the investigated stacks. Dividing the stack's total thickness into a larger number of alternating 1 or 0.5 nm layers, as represented by Stacks #4 and #5, respectively, resulted in better performance than Stack #3 and inferior performance to Stacks #1 and #2. Our findings reveal that when the thickness of each layer in the stack is equal, outstanding surface passivation is obtained, as shown by Stack #2, whereas increasing the thickness of Al_yTiO_x layer in the stack relative to the TiO_x layer is detrimental to passivation performance. This is consistent with the observation for Al_2O_3/TiO_2 stacks that as the Al_2O_3 layer thickness increases, the TiO_2 film has less impact on passivation.[17d] Furthermore, we note that the surface passivation of these stacks was observed to be highly reproducible.

The impact of total stack thickness on surface passivation quality was also explored, as illustrated in Figure 4c,d. As shown in Figure 4d, an ultra-thin stack with a total thickness of 2 nm offers superior surface passivation ($J_0 = 3.9\,fA\,cm^{-2}$) when compared with a pure TiO_2 single layer with a thickness of 2.2 nm ($J_0 = 105\,fA\,cm^{-2}$),[10a] while the highest level of surface passivation was observed for the stack with a total thickness of 4 nm. Further increases in stack thickness resulted in only a marginal increase in the J_0, which could be considered constant within experimental error. This saturation behavior is similar to that previously observed for pure TiO_2.[10a]

Next, we investigated the influence of the precursor sequence as well as the composition of the non-TiO_x layer on the surface passivation quality under identical conditions. For Stack #1 in **Figure 5**a, the ALD process sequence in each supercycle followed the order TMA, H_2O, $TiCl_4$, H_2O (the sequence used elsewhere in this work), while for Stack #2 the sequence was $TiCl_4$, H_2O, TMA, H_2O (i.e., $TiCl_4$ was the first precursor exposed to the Si surface). To form Stack #3, 2 nm of Al_2O_3 was deposited instead of 2 nm of Al_yTiO_x, while Stack #4 replaces the Al_yTiO_x layer with a Hf_yTiO_x layer formed by replacing the trimethylaluminum (TMA) dose step with tetrakis(ethylmethylamido) hafnium (TEMAH) (where the TEMAH dose step was the initial one). The resulting structures are shown schematically in the inset of Figure 5a. Stack #1 with TMA cycle first demonstrated the best performance among the evaluated stacks, as indicated in Figure 5a,b, although the difference with respect to Stack #2 ($TiCl_4$ first) was only slight. Meanwhile, Al-alloyed TiO_x (Al_yTiO_x) (Stacks #1 and #2) outperformed pure Al_2O_3 (Stack #3). Furthermore, when Hf_yTiO_x (Stack #4) was used instead of Al_yTiO_x (Stack #1), the surface passivation quality declined by ≈13 times to $36\,fA\,cm^{-2}$. We conclude that the performance of the Al_yTiO_x layer in the stack is better than the pure Al_2O_3 layer, as shown by Stacks #1 and #2. In addition, Hf in the Hf_yTiO_x layer does not perform the same role as Al in the Al_yTiO_x layer. The reasons behind this are not clear.

Finally, we also investigated how deposition temperature affects the surface passivation and contact resistivity of the optimized stack, Al_yTiO_x/TiO_x. **Figure 6**a shows effective minority carrier lifetime as a function of excess minority carrier density for such stacks deposited at deposition temperatures ranging from 30 to 200 °C. Surface passivation was observed to improve

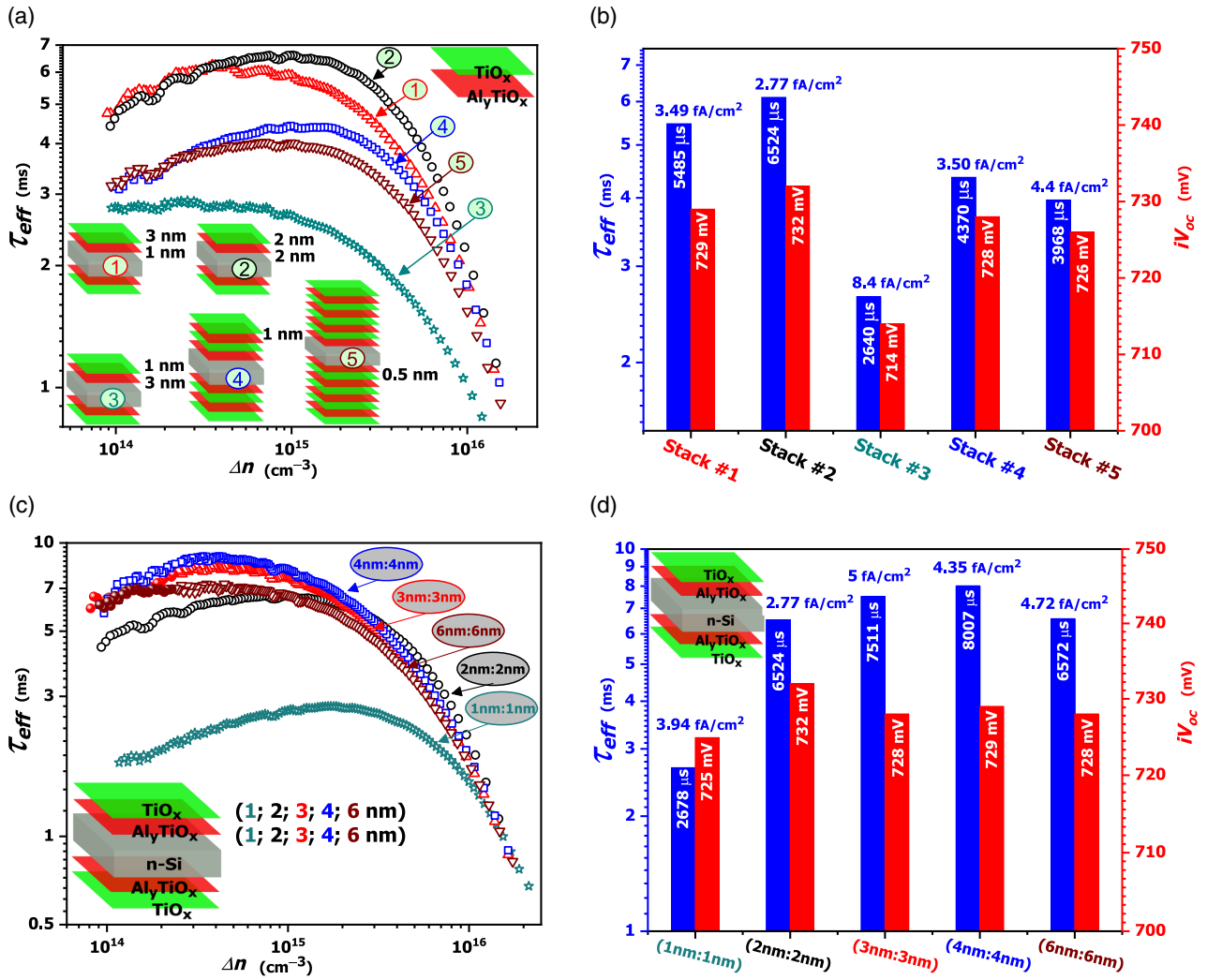

Figure 4. a,c) Injection-dependent effective carrier lifetime of double-side-polished FZ n-type c-Si (286 µm, 2.5 Ω cm) wafers passivated with a) different stacks of TiO_x and Al_yTiO_x with total thickness equal to 4 nm, as represented in the schematic diagrams in this figure, and c) Al_yTiO_x/TiO_x stacks with different total thicknesses where this thickness is equally divided between the layers. b,d) Corresponding variation of the effective minority carrier lifetime and implied open-circuit voltage. All stacks were deposited at 75 °C. The corresponding surface recombination current density prefactors are also written in units of fA cm^{-2}.

somewhat with rising substrate temperature deposition up to 75 °C, before slowly deteriorating above 75 °C, reaching its lowest level at 200 °C. However, iV_{oc} still remained as high as 712 mV, indicating a high level of passivation. In comparison, the passivation of pure ALD TiO_2 deposited from $TiCl_4$ and H_2O is known to degrade dramatically as the substrate temperature increases from 30 to 150 °C.[10a] The variation in τ_{eff} and iV_{oc} of the optimized stack as a function of substrate deposition temperature is represented in Figure 6b, where the values of J_0 and ρ_c are also written. Obviously, 75 °C appears to be the optimal substrate deposition temperature for forming the stack, with outstanding surface passivation ($\tau_{eff} = 6.5$ ms, $iV_{oc} = 732$ mV, and $J_0 = 2.8$ fA cm^{-2}) as well as low contact resistivity ($\rho_c = 23.1$ mΩ cm^2). In a previous study, the effect of deposition temperature on surface passivation was investigated for amorphous TiO_2 deposited on FZ-n-type Si substrates (1 Ω cm) using the same precursors as in our study.[10a] It was reported that the passivation of as-deposited TiO_2 (where the thickness of TiO_2 was not mentioned) reached a maximum value ($\tau_{eff} = 1.1$ ms) at 30 °C and decreased as the temperature increased to a minimum value ($\tau_{eff} = 300$ µs) at 150 °C. These lifetime values correspond to J_0 values between 15.6 and 59.1 fA cm^{-2} for these samples. Consequently, we can conclude that our optimized stack (Al_yTiO_x/TiO_x) of thickness 4 nm outperformed the pure TiO_2 single layer by a factor of ≈4–8 throughout the temperature range (30–200 °C).

The obtained J_0 and ρ_c dependences on the deposition temperature of the novel stack are shown in the inset of Figure 6a. It was observed that increasing the deposition temperature has a detrimental effect on both J_0 and ρ_c characteristics. Crystallization of

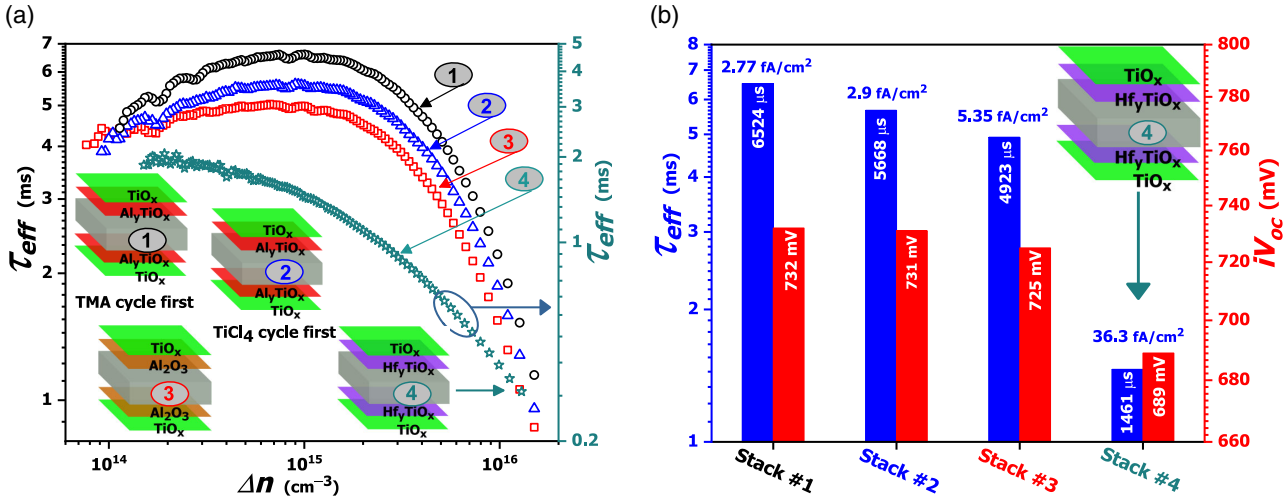

Figure 5. a) Injection level-dependent effective lifetime of double-side-polished FZ n-type c-Si (286 µm, 2.5 Ω cm) wafers passivated with various stacks as represented in the schematic diagrams in this figure and described in the text. All stacks were deposited at 75 °C and the thickness of each layer in the stacks was 2 nm (total stack thickness of 4 nm). b) Corresponding variation of the effective minority carrier lifetime and implied open-circuit voltage. The surface recombination current density prefactor is also given in units of fA cm^{-2}.

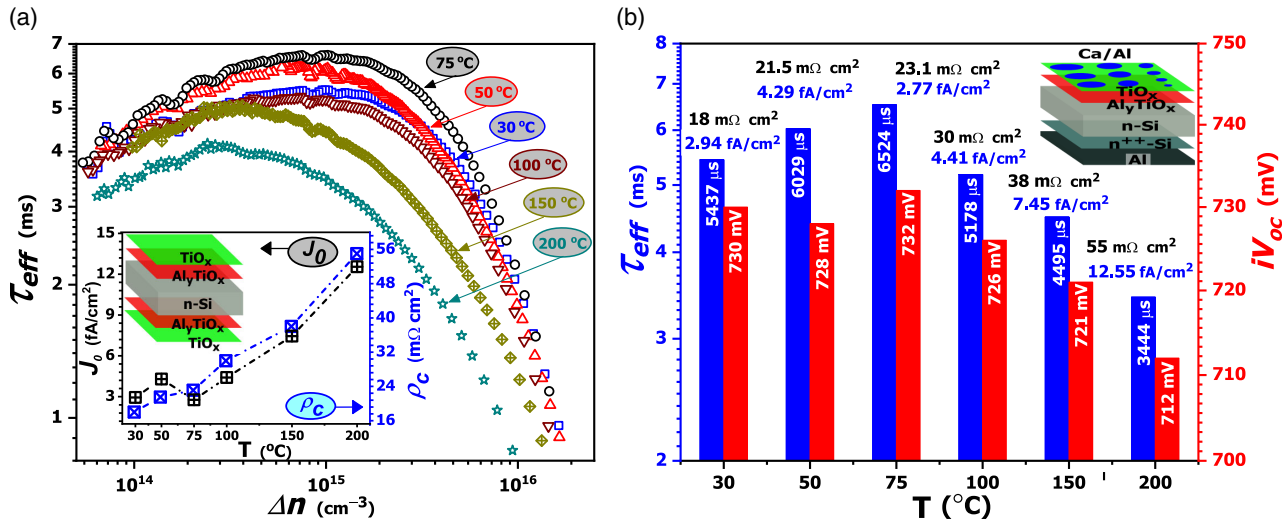

Figure 6. a) Injection level-dependent effective lifetime of double-side-polished FZ n-type c-Si (286 µm, 2.5 Ω cm) wafers passivated with the optimized Al_yTiO_x/TiO_x stack as a function of deposition temperature. For all samples, the thickness of each layer in the stack is 2 nm and the total stack thickness is 4 nm. Inset shows the variation of surface recombination current density prefactor J_0 and contact resistivity ρ_c versus deposition temperature. The inset schematic diagram shows the symmetrical structure used for lifetime tests. b) Corresponding variation of the effective minority carrier lifetime and implied open-circuit voltage of the optimized stack as a function of deposition temperature. The surface recombination current density prefactors and the contact resistivity values are given as well in units of fA cm^{-2} and mΩ cm^2, respectively. The inset shows a schematic diagram of the sample structure used to measure the contact resistivity by the Cox–Strack method.

the stack can be ruled out as an explanation since GIXRD showed that all stacks have an amorphous structure, as shown in Figure S3 (Supporting Information). Interestingly, our results are in line with Suh et al.'s findings regarding the amorphous structure of as-deposited Al_2O_3/TiO_2 stacks at 200 °C.[17d] The fact that surface passivation degradation due to TiO_2 crystallization does not occur in the Al_2O_3/TiO_2 stack upon annealing is a great advantage for this stack in this respect. Therefore, the slight loss in surface passivation (from 2.8 fA cm^{-2} at 30 °C to 12.6 fA cm^{-2} at 200 °C) observed with rising substrate deposition temperature can most likely be linked to the fact that the concentrations of the passivation elements (atomic H and Cl) are reduced with increasing growth temperature. It was previously observed that as the deposition temperature of ALD TiO_2 (using $TiCl_4$ and H_2O precursors as in our study) was increased from 80 °C to 350 °C, the Cl concentration reduced from 2.9 to 0.05 at%. Meanwhile, the hydrogen concentration declined from 2.6 at% at 80 °C to below the detection limit of 0.05 at% at 350 °C.[29]

Although the H (0.4 at%)[29] and Cl (0.3 at%)[29] concentrations may appear to be rather small to accomplish the still-excellent surface passivation of the novel stack at 200 °C, H or Cl may be liberated during layer-by-layer deposition as a consequence of the interaction between surface hydroxyl groups and the titanium precursor $TiCl_4$.[17d] Furthermore, the XPS study (Figure S5c, Supporting Information) indicates that the peak around 199 eV represents residual chlorine in the film (including unreacted chlorine ligands),[31] which may be concentrated at the Si interface and contribute to the passivation mechanism.

Returning to the behavior of contact resistivity as a function of substrate deposition temperature, the cross-sectional transmission electron microscopy (TEM) image of the Al/Ca/stack/n-Si structure deposited at 200 °C was studied to identify whether or not SiO_x formed at the stack/n-Si interface during the deposition process, which could be a contributing factor to the increase in contact resistivity with increasing deposition temperature. As shown in the TEM image in **Figure 7**c, no SiO_x layer is apparent. In addition, the number of ALD cycles was adjusted in accordance with the growth temperature to maintain the thickness of each layer in the stack at 2 nm and the overall stack thickness at 4 nm (using spectroscopic ellipsometry), which is consistent with the thickness identified by TEM. As a result, the potential of a change in stack thickness resulting in a change in contact resistivity with deposition temperature is also ruled out. Therefore, this finding could be attributed to an increase in the bulk resistivity of the stack (e.g., due to a decrease in oxygen vacancy concentrations),[8,32] or an increase in the CBO, or to the possibility of a change in the Al:Ti ratio[33] associated with higher deposition temperatures, all of which would be expected to increase the stack's specific contact resistivity.

2.5. Demonstration in c-Si Solar Cell

Based on Figure 3b, the ESPC enabled by our novel stack (Al_yTiO_x/TiO_x) at 75 °C appears to be highly competitive with state-of-the-art poly-Si ESPCs (SiO_x/n^+-poly-Si), which are currently expected to enable the next generation of c-Si solar cells (while having better optical performance).[34] Therefore, we fabricated front-homojunction c-Si solar cells with full-area rear

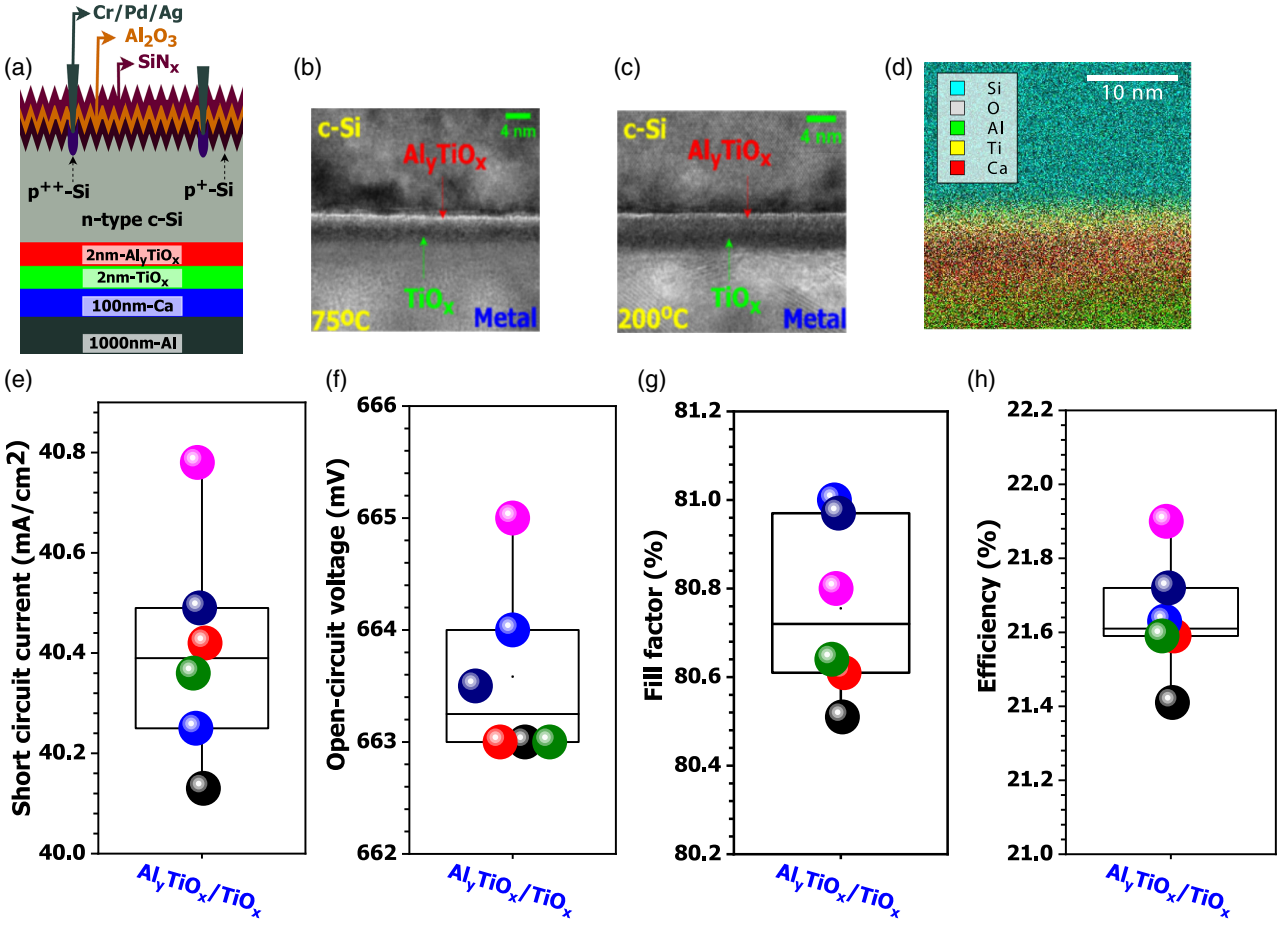

Figure 7. a) Schematic representation of the investigated cell structure with Al_yTiO_x/TiO_x rear contacts, where the Al_yTiO_x/TiO_x stack was deposited at 75 °C. b,c) Cross-sectional TEM images of the c-Si/Al_yTiO_x/TiO_x/Ca/Al interface at 75 and 200 °C, respectively. d) the corresponding EDS mapping of the stack (75 °C deposition). In order to obtain an unobstructed view presenting the stack thickness, the lattice image was collected with the substrate aligned along the $[011]_{Si}$ axis parallel to the $(100)_{Si}$ plane from the Si surface. Solar cell performance statistics with e) short-circuit current, f) open-circuit voltage, g) fill factor, and h) efficiency. Device parameters are obtained from light *J–V* scans under standard test conditions using a solar simulator.

contacts based on Al_yTiO_x/TiO_x/Ca/Al structures, as illustrated in Figure 7a, in order to demonstrate the novel stack performance at a device level. The photovoltaic figures of merit were collected from six cells and their statistical distributions are depicted in Figure 7e–h. The best efficiency among the Al_yTiO_x/TiO_x devices was 21.9% with a short-circuit current $J_{sc} = 40.78\,mA\,cm^{-2}$, an open-circuit voltage $V_{oc} = 665\,mV$, and a fill factor FF = 80.8%. The only moderately high open-circuit voltage of the Al_yTiO_x/TiO_x cells is inconsistent with what would be expected based on the superb surface passivation demonstrated by the novel stack in this study. This suggests that surface passivation deteriorates somewhat following metallization. In a previous work with TiO_2-based contacts,[8,9,35] authors found that the V_{OC} of cells was significantly lower than the implied V_{OC} from lifetime samples, posing a serious challenge for these layers when used as a full-area passivating contact in high-efficiency c-Si solar cells. We note that the efficiency of the c-Si solar cell under investigation, which uses a full-area rear contact of Al_yTiO_x/TiO_x/Ca/Al, is comparable with that of previously reported partial rear-contact device (contact fraction of 6.25%) using TiO_2/Ca/Al contacts, which had a reported efficiency of 21.8%.[35] Furthermore, the best efficiencies have been obtained using pure TiO_2 as a partial rear contact (TiO_2/LiF/Al) with only a very small (≈1%) contact fraction, allowing high efficiency of 23%.[20a] Here LiF potentially also plays a significant role by providing a low WF (achieving ohmic contact and hence low contact resistivity)[36] and suppressing the Al/TiO_x interaction[11] (enhancing the Si surface passivation stability after metallization). Therefore, more research on such stacks is needed to find a strategy to sustain the surface passivation quality after metallization (while still maintaining low contact resistivity) and/or annealing so that they can be applied as full-area ESPCs in high-efficiency devices and be compatible with the high-temperature processes required in the production of c-Si solar cells. Indeed, our initial result using the novel stack at the device level is highly encouraging, and we expect to improve upon it in subsequent iterations by addressing the issue of passivation stability following metallization, which is a common issue for passivating contacts. Finally, we believe that by definitively addressing these challenges, our novel stack has the potential to match, and possibly outperform, Si-based contacts (a-Si:H and poly-Si) in terms of fabrication cost, simplicity, and performance.

3. Conclusion

A comprehensive optimization of Al-alloyed and pure TiO_x layers and stacks as ESPCs for application in c-Si solar cells has been presented. Outstanding surface passivation ($J_0 < 3\,fA\,cm^{-2}$) combined with low contact resistivity ($\rho_c < 20\,m\Omega\,cm^2$) is demonstrated using a novel Al_yTiO_x/TiO_x stack. The passivation performance in particular is significantly better than previously reported for passivating contacts based on TiO_2 or other metal oxides and in fact is comparable with that of state-of-the-art SiO_x/n^+-poly-Si stacks. An efficiency of 21.9% with a short-circuit current $J_{sc} = 40.78\,mA\,cm^{-2}$, an open-circuit voltage $V_{oc} = 665\,mV$, and a FF = 80.8% has been achieved for proof-of-concept n-type c-Si solar cells featuring a full-area Al_yTiO_x/TiO_x-based contact. This study establishes a pathway for the development of novel heterocontacts combining outstanding electrical properties with high optical transparency, capable of addressing current performance limitations in high-efficiency c-Si solar cells, based on Earth-abundant, economical, and simple-to-prepare TMOs that are appropriate for industrial use.

4. Experimental Section

Sample Preparation and Characterization: ALD (Beneq TFS 200, Finland) was used to deposit Al-alloyed TiO_x (Al_yTiO_x) and pure TiO_x single layers and stacks following the recipe shown in **Figure 8**a. The precursors used in this study were titanium chloride ($TiCl_4$) and trimethylaluminum (TMA, $Al(CH_3)_3$). Tetrakis(ethylmethylamido) hafnium (TEMAH) was used in place of TMA to deposit Hf-alloyed TiO_x layers. Deionized water was used as an oxidant and high-purity nitrogen (99.999%) as a purge gas.

The film thickness was determined via spectroscopic ellipsometry measurements (J.A. Woollam M2000D, USA) by fitting polarized reflectance data on single-side-polished silicon substrates. GIXRD patterns were performed using a diffractometer with Cu Kα radiation ($\lambda = 1.5418$ Å) source (Hi-resolution PANalytical X'Pert PRO MRD system) operated at 45 kV and 40 mA. Diffraction patterns were recorded automatically with a scanning speed of $2°\,min^{-1}$ from 10° to 100° for samples deposited on double-side-polished FZ (100) n-type crystalline silicon (c-Si) substrates. XPS, UPS, and inverse photoemission spectroscopy (IPES) were conducted to determine the elemental compositions, WFs, and valence and conduction band energies of the films. XPS was conducted in an ultra-high-vacuum (UHV) apparatus from SPECS, with a base pressure at a few 10^{-10} mbar. An Mg-Kα line (12 kV, 200 W) from a nonmonochromatic X-ray source was used for the measurements.[37] A survey scan at pass energy of 40 eV was processed first. High-resolution scans at pass energy of 10 eV were then recorded for Ti, Al, Cl, O, and C. The energy scale of the XPS spectra was not calibrated because the C–C sp^3 was found within the error bar of ±0.15 from 285 eV and the charging of samples did not present. It should be noted that the C present at the surface of the sample is from adventitious hydrocarbons which are present at any surface unless the surface has been treated specifically under UHV to remove these adventitious hydrocarbons. UPS was applied to determine the occupied electron states of the sample surface (valence electron states) and the minimum energy required for an electron to escape the surface (secondary electron for WF).[38] In the measurement, electrons were emitted under UV radiation of 21.22 eV excitation energy. The UPS was operated in situ with XPS to avoid any contamination during sample transfer. IPES was used to determine the unoccupied electron states (conduction electron states) of a sample based on an electron in/photon out mechanism. In the experiment, a beam of electrons with specified energy was directed onto the sample surface, entering the unoccupied states and releasing photons with corresponding energy.[39] The photon was detected by the ionizing gas phase of an Ar/acetone mixture inside a Geiger–Müller tube. The emitted photons were collected as a function of the kinetic energy of the electrons to compose the IPE spectrum. By operating in situ IPES after UPS, a complete energy band structure of the sample could be obtained. For determining the WF, the secondary-electron cutoff on the binding energy scale of the UPS spectra was analyzed. The WF was found by calculating the difference between the excitation energy of UV light, which was 21.22 eV for UPS, and the secondary-electron cutoff along the baseline of the spectra. The value of the valence band energy was determined by approximating the baseline and the onset of valence electron emission of UPS with linear fits and determining their intersections. The same procedure was applied for determining the value of the conduction band energy from the onset of the IPES spectra. When quantifying the peaks of XPS spectra, the intensity of peaks of various elements was normalized using an atomic sensitivity factor (ASF).[40] A Zeiss Crossbeam 550 Ga dual beam was used to obtain the TEM lamellae used for the cross-sectional observations presented in this study. The final polishing of the specimen was carried out with the Ga acceleration voltage set for 5 kV. The TEM images were obtained using a JEOL 2100F system

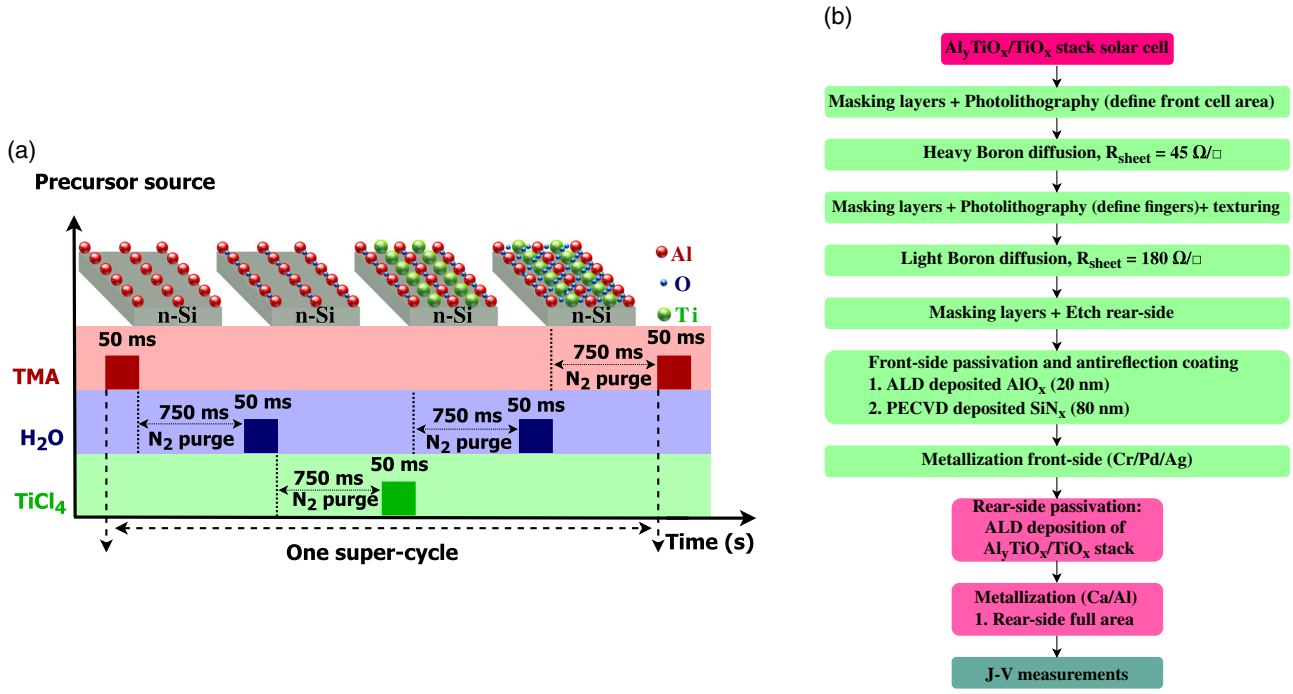

Figure 8. a) Schematic diagram of the ALD supercycle sequence used for the deposition of the Al-alloyed TiO_x (Al_yTiO_x) layers. Al, Ti, and O atoms are schematically represented by red, green, and blue spheres. Each precursor or reactant pulse lasts 50 ms and is followed by 750 ms of N_2 purging. Al, O, and Ti species coexist within the same atomic monolayer after finishing one supercycle. b) Process sequence with the main steps for the fabrication of n-type c-Si solar cells with a full-area rear contact based on Al_yTiO_x/TiO_x stacks.

operating at 200 kV. The EDS elemental maps were acquired in scanning transmission electron microscopy (STEM) mode using the high resolution transmission electron microscopy (HRTEM) for an n-Si/Al_yTiO_x/TiO_x/Ca/Al structure.

Three types of Si substrates were used: 1) planar Cz (100) 7–10 Ω cm n-type with a thickness of 105 µm; 2) double-side-polished FZ (100) 2.5 Ω cm n-type with a thickness of 285 µm for surface passivation studies, and 3) planar Cz (100) ≈1 Ω cm n-type c-Si substrates with a thickness of ≈165 µm for contact resistivity measurements. Initially, all planar Cz n-type Si wafers used in this study were etched in 25 wt% tetramethylammonium hydroxide (TMAH) at 70 °C for 5 min to remove any saw damage followed by a standard Radio Corporation of America (RCA) cleaning process[41] and 1% – 2% HF (hydrofluoric acid) solution dip. Subsequently, tabula rasa[42] (at 1050 °C for 1 h in a quartz tube furnace) and gettering treatments (at 880 °C for 40 min using liquid $POCl_3$ precursor in a Tempress S5T1 tube furnace) were performed to improve the bulk quality of the planar Cz Si substrates. The double-side-polished FZ n-type c-Si substrates were used as received without any high-temperature treatment. All wafers were then RCA cleaned and dipped in dilute 1 – 2% HF for 30 s to remove any native oxide immediately prior to all ALD depositions. Contact resistivity was measured by the Cox–Strack method[19] on samples processed as shown in the schematic diagrams in Figure S1 (Supporting Information).

Current–voltage (*I–V*) measurements for contact resistivity samples were performed at room temperature in the dark using a Keithley 2425 source meter. Surface passivation was characterized using a Sinton Instruments WCT-120 photoconductance lifetime tester. Surface recombination current density prefactor J_0 was determined via the method of Kane and Swanson,[43] using the intrinsic lifetime parameterization of Richter et al.,[44] and a value of 8.6×10^9 cm^{-3} for the intrinsic carrier concentration.

Device Fabrication and Characterization: Small-area cells (2 cm × 2 cm) with full-area rear contacts Al_yTiO_x/TiO_x stacks were fabricated on n-type c-Si substrates (1 Ω cm, 200 µm). The process sequence to fabricate these cells is also illustrated in Figure 8b. *J–V* measurements were performed using a solar simulator system (WAVELABS Solar Metrology Systems GmbH) with no preconditioning protocol under standard test conditions (AM 1.5G, 1000 W m^{-2}, 25 °C). The light intensity was calibrated before the measurements using a certified Fraunhofer CalLab reference cell.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the Australian Renewable Energy Agency (ARENA) through the Australian Centre for Advanced Photovoltaics (ACAP). This work was made possible through access to the ACT node of the Australian National Fabrication Facility (ANFF-ACT). The authors acknowledge the facilities and the scientific and technical assistance, of Flinders Microscopy and Microanalysis (formally known as FMMA) and the South Australia node of the Australian National Fabrication Facility (ANFF-SA) for conducting the XPS and UPS analysis. The authors would like to express their gratitude to Frank Brink for assisting in the focused ion beam transmission electron microscopy sample preparation.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

high efficiencies, passivating contacts, photovoltaics, silicon solar cells, silicon surface passivation, TiO_2, transparent electron-selective contacts

Received: June 20, 2022
Revised: July 22, 2022
Published online: August 16, 2022

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