

MATERIALS SCIENCE

Nonvolatile ferroelectric domain wall memory

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Ferroelectric domain walls are atomically sharp topological defects that separate regions of uniform polarization. The discovery of electrical conductivity in specific types of walls gave rise to “domain wall nanoelectronics,” a technology in which the wall (rather than the domain) stores information. This paradigm shift critically hinges on precise nanoengineering of reconfigurable domain walls. Using specially designed nanofabricated electrodes and scanning probe techniques, we demonstrate a prototype nonvolatile ferroelectric domain wall memory, scalable to below 100 nm, whose binary state is defined by the existence or absence of conductive walls. The device can be read out nondestructively at moderate voltages (<3 V), exhibits relatively high OFF-ON ratios ($\sim 10^3$) with excellent endurance and retention characteristics, and has multilevel data storage capacity. Our work thus constitutes an important step toward integrated nanoscale ferroelectric domain wall memory devices.

INTRODUCTION

In recent years, there has been a strong surge in investments toward alternative disruptive technologies to meet increasing demands for fast high-density, nonvolatile data storage and logic devices (1, 2). For example, in “racetrack memories,” high-density digital information is encoded in the form of magnetic domain walls (DWs) controllably injected and moved along three-dimensional (3D) ferromagnetic nanowires using spin-polarized electric currents (3, 4). An analogous pathway in ferroelectric materials is of tremendous current interest (5). Ferroelectric DWs (FEDWs) are one to two orders of magnitude sharper than their magnetic counterparts (5), thereby promising much higher storage densities. In principle, FEDWs can be readily written, erased, rewritten, and displaced on demand by an applied electric field, bestowing upon them marked advantages over their ferromagnetic counterparts in terms of selective writing, scaling, speed, and energy consumption (5). Reconfigurable FEDWs could one day deliver the promise of “now you see it, now you don’t” adaptive circuitry, a principal requirement of future neural network architectures (6). The question then is: How can one exploit FEDWs for nanoelectronic functionalities? The direct experimental demonstration of enhanced conductivity at specific DWs in otherwise insulating ferroelectric oxides (7–10) led to the idea that a FEDW, rather than the domain itself, can store information. Following this initial discovery, DW conductivity has been unambiguously identified in several other ferroelectrics (11–14). Although conductive FEDWs were predicted as far back as the 1970s (15), critical advances made recently in the understanding of their nature and conduction properties (14–22) have enabled the knowledge required to realize FEDW memory and logic devices based on these nanoscale elements (23–27). For example, the ability to precisely manipulate FEDW conductivity (14, 18–21), modulate and gate FEDW transport (23–27), and create FEDW interconnects have been pivotal milestones toward the development of a

functioning memory. However, despite these accomplishments, and although nonvolatile, solid-state ferromagnetic DW memory is now nearly mature enough for commercialization (3, 4), even a simple two-terminal prototype FEDW memory has yet to be demonstrated.

Here, we demonstrate a two-terminal prototype scalable (sub-100 nm) nonvolatile FEDW memory with high OFF-ON ratio ($\geq 10^3$), excellent retention (10^4 s), and robust endurance ($\sim 10^3$ cycles) characteristics. This achievement is made possible through a combination of electron beam (e-beam) nanolithography, judicious selection of the crystallographic growth direction of high-quality epitaxial bismuth ferrite thin films and custom-designed scanning probe microscopy (SPM) approaches. In particular, the specially designed in-plane geometry of the electrodes allows for encoding and retrieval of information via moderate electric fields rather than electric currents, thus enabling low-energy operation. The low-voltage, pulse-based readout of the written states is nondestructive. Furthermore, the reconfigurable FEDWs enable a possibility of achieving multilevel data storage; a series of sequentially distinct resistance states can be tuned in a stepwise manner via precise control of DW length. Therefore, data storage densities of these FEDW memory devices can be improved markedly compared to what is achievable using traditional binary bits.

RESULTS

High-quality epitaxial BiFeO₃ (BFO) thin films were grown on (110) SrTiO₃ (STO) substrates using pulsed laser deposition (details in fig. S1). (110)-oriented BFO thin films can display an almost monodomain character in their as-grown state (28) and thus provides for a clean template to inject and erase DWs. Using e-beam nanolithography, Pt/Ti coplanar geometry metal electrodes were patterned (schematic of Fig. 1A and fig. S2), enabling the application of an electric field in the plane of the film. This electrode geometry is crucial because the application of bias between the electrodes can induce switching between the two naturally occurring ferroelastic domain variants of the (110)-oriented BFO film (28, 29). Both the interelectrode spacing and the lateral size of one electrode were restricted to a few hundreds of nanometers to enable relatively low-bias operation and controlled nucleation of an isolated DW pair (Fig. 1B and fig. S3). In this geometry, the large metal electrode was grounded, whereas the writing or the switching bias, used to realize a specific FEDW configuration, was supplied by placing a conductive atomic force microscopy (c-AFM) tip in contact with the small metal electrode. This is a fundamental

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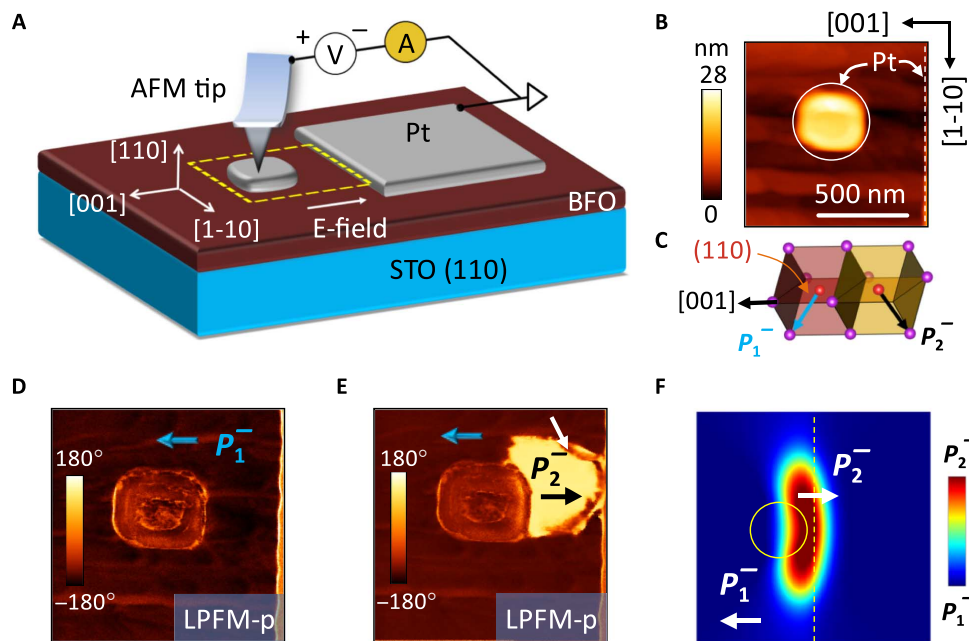


Fig. 1. Experimental geometry and details of the ferroelectric switching process. (A) Schematic of the experimental geometry for investigation of the prototype FEDW device. E-field, electric field. (B) Topographic image of the actual e-beam-fabricated device on the surface of the BFO thin film acquired over the dashed square-frame area, as shown in (A). (C) Schematic showing two polarization variants separated by 71° between the neighboring unit cells (purple, Bi atom; red, Fe atom). (D) LPFM phase image of the as-grown state of the BFO thin film corresponding to the topographic image displayed in (B). (E) LPFM phase image acquired after application of coplanar switching field between the metal electrodes. (F) Phase-field simulation of the switched ferroelastic domain in equilibrium. In (B) and (F), the enclosed circular frame represents small metal electrode, and the dashed vertical straight line represents boundary of large metal electrode. Images in (D) and (E) were acquired with the long axis of the cantilever being oriented along the $[-110]$ direction.

and significant change from previous FEDW engineering reports that exploited in-plane geometry of electrodes (23, 29–31). Full details of the patterning process are given in fig. S2. In Fig. 1B, one can discern the typical stripe-textured morphology of the (110)-oriented BFO film, the direction along which the in-plane component of the ferroelectric polarization arises (Fig. 1C). To induce switching, the in-plane electrodes were oriented parallel to these morphological stripes. The operational characteristics of the two-terminal device thus fabricated were probed using SPM methods. Specifically, piezoresponse force microscopy (PFM) was used for high-resolution visualization of the domains and DWs, as well as details of the ferroelectric switching processes. Electrical transport characteristics of the devices were investigated by c-AFM.

We begin with PFM imaging, performed over an area shown by the dashed square region in Fig. 1A corresponding to the topographic image in Fig. 1B. Both in-plane [lateral PFM (LPFM)] and out-of-plane [vertical PFM (VPFM)] 2D PFM images were acquired. We follow the nomenclature used by Cruz *et al.* (28). In the as-grown film (Fig. 1D), the uniform contrast in the acquired LPFM (VPFM; fig. S4) phase image attests that we clearly have a monodomain state over the captured area. The typical as-grown state of (110)-oriented BFO films comprises two polarization variants (P_1^- and P_2^- ; see Fig. 1C and fig. S5) pointing toward the bottom interface separated by 71° with predominance ($P_1^- \gg P_2^-$) of one over the other (28, 29). The presence of two ferroelastic domain variants is confirmed by the observed splitting of the (221) BFO peak along the $[110]_{\text{pseudocubic}}$ direction from the acquired x-ray diffraction reciprocal space map (fig. S1). The intensity of one of the split (221) BFO peaks is one order of magnitude larger than the other, validating the predominance of a

single ferroelastic domain variant in agreement with the PFM imaging results. Next, to initiate ferroelectric switching and create FEDWs between the metal electrodes, we applied a coplanar switching bias (electric field pointing from left to right) of sufficiently high magnitude (+8 V) between the metal electrodes. It is emphasized that the FEDWs are reconfigured through switching of the ferroelectric domains (fig. S6). The application of the switching bias resulted in the creation of a pair of FEDWs and an enclosed domain of opposite in-plane polarity with a triangular shape (Fig. 1E). At the same time, the out-of-plane polarization component remains unchanged (fig. S4). This can be understood in terms of rotation of the polarization vector by 71° from P_1^- to P_2^- (Fig. 1C) such that the in-plane component of the polarization flips along the $[001]$ direction (fig. S5), whereas the out-of-plane component of the polarization remains oriented downward (figs. S4 and S7). Phase-field simulations (Fig. 1F) agree with the experimentally observed switching process and corroborate the strategy based on experimental configuration for the control of FEDWs (details in fig. S8). Thus, the application of a coplanar switching field results in purely ferroelastic switching and leads to the creation of 71° FEDWs between the metal electrodes. This underlines the importance of choosing the right crystallographic orientation in BFO thin films. Note the characteristic overall triangular shape of the switched ferroelastic domain (Fig. 1E), which agrees reasonably well with the simulated domain profile (Fig. 1F). The switched domain can appear with sharp or rather diffuse triangular (arrow-like) facets especially toward the end where it meets the counter large metal electrode (see figs. S9 and S10). This characteristic shape, discussed previously (28), is a result of the interplay between epitaxial mechanical constraint and electrostatic depolarization fields.

Moreover, domain configurations can be highly complex and may not be resolved fully by the PFM measurements alone. This is especially true for variations in the polarization configuration through the thickness of the film, which can be elucidated using techniques such as spherical aberration-corrected transmission electron microscopy (27, 32).

One fascinating aspect of the switching process is the formation of an arrowhead-shaped domain (dark-color domain pointed by a white arrow; Fig. 1E) of a polarity opposite to the applied switching field direction. The intriguing fine-stripe domain of opposite polarity is a common occurrence rather than an anomaly and is resolved quite cleanly in our measurements (see figs. S9 and S10) (33). The formation of this domain, of a width of about 25 nm, near the end of the switched (yellowish) ferroelastic domain leads to an arrangement of closely spaced charged arrowhead FEDWs of alternate polarity as one moves from the large metal electrode toward the smaller electrode. Here, the FEDW charge sequence goes as head-to-head to

tail-to-tail and finally to head-to-head. A full description of this process will be reported elsewhere. Nonetheless, the 71° FEDWs were controllably injected, erased, and reinjected (transformation shown in Fig. 1, D and E) repeatedly between the metal electrodes. Critically, the written FEDW states were confirmed to be stable, thus encouraging further probing of the FEDW transport behavior.

Having established that stable FEDWs can be injected and erased, we next investigated the memory characteristics of the device. To do so, first FEDWs were written (Fig. 2A) such that the FEDWs bridged the two coplanar metal electrodes. Thereafter, noninvasive current mapping (at biases lower than the switching biases) was performed to read the resistance state and, importantly, to visualize electrical conductivity paths. Figure 2 (B to D) presents a series of current maps acquired at specific increments of dc bias. The maps clearly show high electrical conduction through the 71° FEDWs only, whereas the domains themselves exhibit negligible conduction. As a result of the

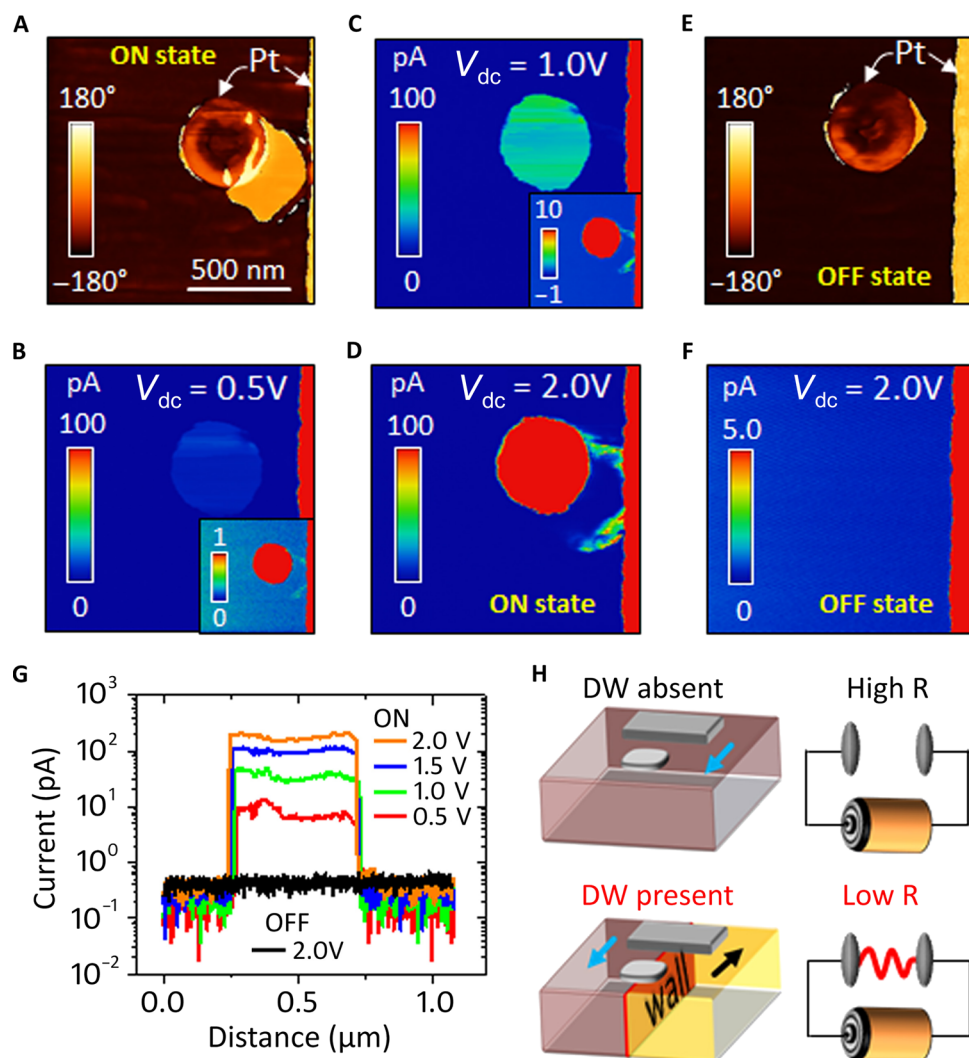


Fig. 2. Demonstration of working principle of the FEDW memory. (A) LPFM phase image acquired after creation of FEDWs between metal electrodes. (B to D) c-AFM images acquired corresponding to DW configuration in (A) at a fixed dc bias of +0.5 V (B), +1.0 V (C), and +2.0 V (D), respectively. Insets in (B) and (C) show the same c-AFM image over a reduced range of the color scale bar. (E) LPFM phase image acquired after erasure of FEDWs between the metal electrodes. (F) c-AFM image acquired corresponding to FEDW configuration in (E) at a fixed dc bias of +2.0 V. (G) Cross-section profile of the c-AFM images in (B) to (D) and (F) across small metal electrode along the vertical direction. (H) Schematic showing working principle of the FEDW memory.

presence of highly conducting DWs between the metal electrodes, the FEDW device exhibits a low-resistance state, evidenced by the high electrical current measured between the electrodes (that is, when the tip is over the small electrode). This is manifested as the bright annular contrast in the small metal electrode in the corresponding current map (Fig. 2, B to D). Next, a FEDW-free state is created by applying a switching bias (-8 V) in the opposite polarity. The LPFM image (Fig. 2E) acquired thereafter confirms the erasure of the FEDWs between the metal electrodes. Now, the corresponding *c*-AFM map (Fig. 2F) for the FEDW-free state reveals negligible conduction levels (that is, ~ 100 fA), thus establishing the presence of a high-resistance state. Cross-section profiles (across the small metal electrode along the vertical direction) acquired for the current maps in conductive and resistive states shed further light. As shown (Fig. 2G), the presence of FEDWs (the ON state) results in a uniform electrical current across the metallic electrode, increasing in magnitude with a corresponding increase in the read bias, whereas the FEDW-free state (OFF state) shows very low levels of electrical current. The uniform nature confirms (i) the absence of contributions from the polarization switching and/or relaxation current and (ii) that the observations are free from tip-electrode edge-effect complexities. This agrees with no discernible changes observed in the FEDW configuration before and after the *c*-AFM measurements. Further, the cross-section profiles reveal a relatively high-resistance contrast of about three orders of magnitude between OFF and ON states (at a read bias of $+2$ V). These results therefore unequivocally demonstrate the concept of a two-terminal nonvolatile FEDW memory whose operation is linked to the presence or absence of 2D conducting FEDWs (Fig. 2H). In the presence of a conducting FEDW channel connecting the spatially separated in-plane metal electrodes, a low-resistance state is realized (ON state). The FEDW interconnect provides a low-resistance pathway for electrical current (measured noninvasively) between the spatially separated in-plane metal electrodes. Upon erasure of the conducting FEDW channel (that is, the absence of FEDW) between the spatially separated metal electrodes, a high-resistance state is achieved (OFF state) because the ferroelectric material in the absence of FEDWs is a poor conductor of electricity. The FEDW memory is resistive in nature. In FEDW memory, the encoded state (that is, DW present or absent) is read by measuring the net resistance noninvasively between the spatially separated in-plane metal electrodes (Fig. 2H). For our prototype FEDW device, the writing operation (6 to 8 V) is performed at moderate biases, whereas the current-based readout of the written states is at much lower biases of ~ 2 V. Note that the read operation is nondestructive unlike traditional ferroelectric random-access memory (FeRAM) (1, 2, 34).

To gain further insight into the electrical transport characteristics of the prototype FEDW memory, we performed spectroscopic current-bias measurements in the noninvasive bias regime (± 2 V) between the electrodes in the presence (ON state) and absence (OFF state) of DWs for a number of these prototype devices (Fig. 3, A and B). The acquired current-bias (*I*-*V*) curves for the ON state show high electrical conduction and are nearly symmetric, as expected for similar metal electrodes (7). In contrast for the OFF state, electrical conduction is extremely low with little or no variation for the acquired curves. Thus, the spectroscopic current-bias measurements agree with the imaging results shown in Fig. 2 and further demonstrate the reproducibility of OFF and ON states with relatively high-resistance contrast (that is, OFF-ON ratio $\geq 10^3$). The retention and endurance characteristics of the prototype FEDW memory device are shown in Fig. 3

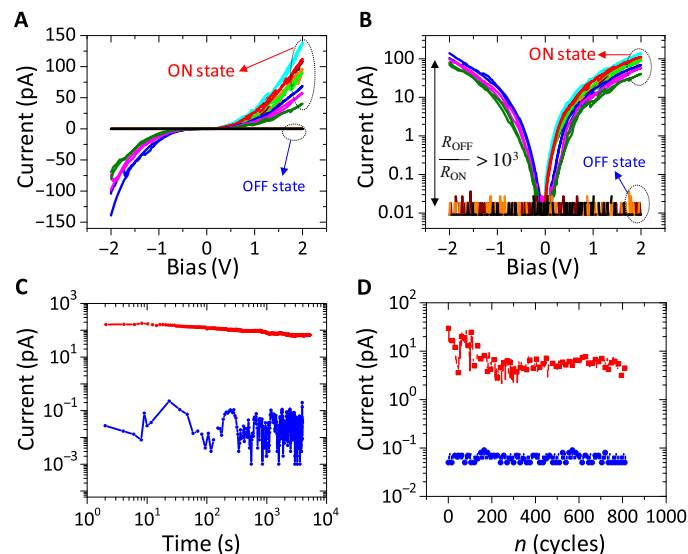


Fig. 3. Transport, retention, and endurance characteristics of the FEDW memory. (A) Spectroscopic current-bias curves acquired for the OFF and ON states of FEDW memory devices. (B) Same plot as in (A) but with a logarithmic y scale. (C) Time dependence of the written OFF and ON states of the FEDW memory acquired at a read bias of $+2.0$ V. (D) Endurance characteristics of the FEDW memory device.

(C and D). The states are encoded by applying bias pulses of amplitude in the range of 6 to 8 V and a duration of 1 s. The encoded state is read noninvasively via measuring electrical current at read bias pulses of an amplitude of 2 V and a duration of 1 s. The retention measurements probe the stability of the written states, whereas the endurance measurements investigate the fatigue or the repeated switchability between OFF and ON states. The time-dependent measurements clearly demonstrate the relative long-term stability and nonvolatile character of the written binary OFF-ON states. On the other hand, the endurance measurements show repeated switchability, maintaining a sufficiently high-resistance contrast between OFF and ON states over nearly 10^3 cycles. Beyond 10^3 cycles, the *c*-AFM tip degraded considerably, suggesting that this limit is not because of the FEDW fatigue itself.

The final part of the study focuses on the possibility to implement multilevel data storage. Thus far, we have demonstrated nonvolatile but solely binary data storage capabilities (that is, OFF and ON states) similar to FeRAMs (34). An additional defining characteristic of FEDWs that can be exploited to further enhance the potential of these devices is the dynamic nature of their electrical conduction (9). The FEDWs are not rigid conductors, and as a consequence, the overall resistance of these 2D sheets is expected to change as a function of their length. This is already noticeable in Fig. 2 (B to D), where the conductivity profile along the FEDW decreases as a function of its increasing length from the large metal electrode. The conduction profile along the DW decreases because of increasing sheet resistance between the tip and the large metal electrode. This means that the resistance level or state of the FEDW memory device can be tuned as a function of the FEDW length between the coplanar metal electrodes. Although this can be achieved by applying writing bias pulses of finely tuned magnitude and durations, an alternative, more direct approach, however, is to vary the spacing between the metal electrodes. The varying spacing between the metal electrodes sets the average

FEDW length to be equal to the spacing itself. Using this approach (Fig. 4, A to F), we have realized FEDWs of different lengths ranging from about 400 to 90 nm, which bridge the in-plane metal electrodes. The corresponding current maps (Fig. 4, A to F) reveal a stepwise change in the resistance level of the devices as a function of FEDW length. As shown (Fig. 4, G and H), the resistance level changes from a high-resistance state (R_1) to an intermediate-resistance state (R_2) and finally to a low-resistance state (R_3) as a function of decreasing FEDW length between the metal electrodes. The resistance level of the FEDW memory varies nearly exponentially as a function of average DW length between the metal electrodes (Fig. 4H; note the log scale of the y axis). Thus, nanoscale changes in the DW length lead to quite large changes in the resulting electrical current or resistance state of the device. Another interesting aspect (Fig. 4, A and B) is that it is not even necessary to erase FEDWs to transition to an OFF state; this is possible along with a spectrum of distinct low-resistance-level states by tuning the FEDW length. Hence, the resistance level of the FEDW memory can be tuned in a sequential and stepwise manner to achieve multilevel data storage via the precise nanoscale control of the DW length. Therefore, data storage densities of these FEDW memory devices can be improved markedly compared to what is conventionally achievable with just binary logic.

Besides DW length, relative fractions of charged versus uncharged DW segments are also an important consideration (27), which can explain the behavior observed in Fig. 4H. At a spacing of ~ 400 nm (Fig. 4, A and B) between the metal electrodes, the fraction of nominally uncharged DW segments is greater compared to that of the charged DW segments. However, at this length scale (~ 400 nm), the conduction level of the device will remain unchanged within the resolution limit of the current measuring setup even if charged DW segments are replaced by the uncharged DW segments. Therefore, the DW length is a primary factor in determining the conduction level of the device at this length scale. As shown in Fig. 4 (A and B), charged DW segments appear with the following characteristic features: (i) a significant tilt from a straight-line configuration (for example, the DW segment at the top near the large metal electrode in Fig. 4A) and (ii) enhanced electrical conduction observed for the charged DW segment (from the c-AFM map in Fig. 4B; charged DW segment appears with red contrast, indicating increased conduction). Now, with decreasing spacing between the in-plane metal electrodes (Fig. 4, C to F), the DWs are nominally uncharged because the characteristic features noted above for the charged wall segments are missing. This is because the DWs in Fig. 4 (C to F) are not significantly tilted and appear as a more or less straight line. The conduction along the DWs in

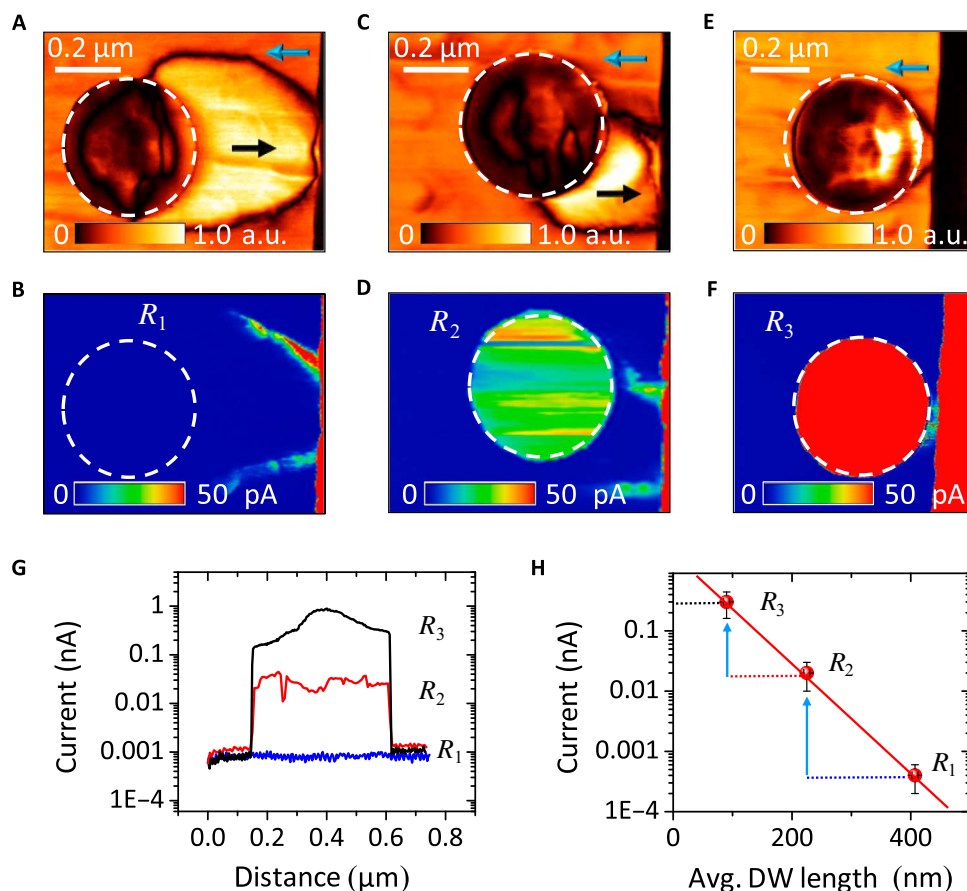


Fig. 4. Multilevel resistance states of the FEDW memory. (A to F) LPFM amplitude (A, C, and E) and the corresponding c-AFM images (B, D, and F) as the spacing between coplanar metal electrodes changes from 407 nm (A and B) to 225 nm (C and D) and finally to 90 nm (E and F), respectively, for the prototype FEDW memory devices. a.u., arbitrary units. (G) Cross-section profile of the c-AFM images (B, D, and F) across the small metal electrode (shown by the dashed circle) along the vertical direction. (H) Plot of the measured electrical current between the electrodes as a function of corresponding average DW length. The red line in (H) represents the exponential dependence of the electrical conduction on FEDW length. The c-AFM maps were acquired noninvasively at a fixed dc read bias of +2.0 V.

Fig. 4 (C to F) is relatively lower than the one seen for the charged DW segment in Fig. 4B (note that the range of the color scale is the same for all *c*-AFM images in Fig. 4) at similar distances from the large metal electrode. Therefore, we argue that, in these particular instances presented in Fig. 4, the DW length is a primary factor, but this may not always be the case, and charged versus uncharged DW fractions might be a predominant factor in other cases (27).

Furthermore, the findings presented in Fig. 4 also illustrate the highly scalable nature of FEDW memory devices. The OFF-ON ratio for the FEDW memory increases from about 1 to 10^3 with decreasing lateral length scale (Fig. 4). The data presented in Fig. 4 (E and F) demonstrate the sub-100-nm operation of the FEDW memory (fig. S11). There is thus significant potential for further scaling down of the FEDW memory by one to two orders of magnitude because, in principle, it is possible to realize DWs at the sub-10-nm length scale (5). In addition, we would like to note that the out-of-plane component of polarization remains unaffected in the sub-100-nm FEDW device (Fig. 4, E and F), and the spatial separation between the electrodes is still approximately two times the thickness (~ 53 nm; fig. S1) of the ferroelectric film. Thus, the electric field is predominantly in the plane, in agreement with theoretical finite element calculations (fig. S12). Currents are measured in-plane; thus, the in-plane components of the electric field are the driving force for any measured current in our devices.

DISCUSSION

The performance of FEDW memory and observed nonlinearities in the measured transport characteristics (Figs. 3A and 4) merit further discussion. First, the nonlinear *I*-*V* curves (Fig. 3A) measured between the spatially separated metal electrodes in the presence of a FEDW interconnect can arise from a variety of factors at play, examples of which include non-ohmic contacts (7, 10), shape of the electric field (nonuniform field distribution between metal electrodes), and non-metallic intrinsic conductivity behavior of the FEDWs. In recent reports (20, 21), metal-like conduction behavior has been observed for bent and charged FEDWs; however, the universality of this phenomenon remains to be established. For nonlinear conductivity profile along FEDW (Figs. 2 and 4), the effect of tip-sample contact can be excluded because it more or less remains the same as the same tip moves along the FEDW length. The nonlinear behavior in this case likely arises from a nonlinear dependence of the probe electric field distribution with increasing distance along the FEDW, besides a contribution from pathways (other than the shortest distance in the in-plane) along the DW plane into the depth of the sample. The net electrical current measured between the tip and large metal electrode is an integral of electrical current over all the possible paths on the plane of the FEDW. However, the predominant contribution will be from the shortest in-plane path.

Next, we make few observations about the performance of the FEDW memory. Although some of the important characteristics of FEDW memory are quite impressive (that is, OFF-ON ratio, non-volatile nature, scalability, and multilevel data storage), a few characteristics such as the speed of the read/write operation and amplitude of the writing bias pulses to encode states need to be improved further to enable fast ultralow bias operation. Options include choosing alternative suitable materials or new design strategies. For example, decreasing the lateral spacing between the in-plane electrodes (between the nanopatterned electrodes) will lead to sufficiently strong

electric fields needed to write or erase FEDWs even at small biases. Alternatively, defect engineering to create regions of enhanced field strengths, so-called “hot spots” at certain locations in the ferroelectric thin films (23), can also be used to further reduce the writing biases/time scales needed to encode states in FEDW memory. We note that, in the case of relatively long FEDW interconnects (~ 400 nm; Fig. 4, A and B), the problem associated with readout of encoded states becomes highly pronounced. The electrical current (measured at low read bias) in the presence and absence of FEDWs is nearly indistinguishable within the resolution of our current measuring setup (~ 100 fA) due to a very small value of the electrical current. An obvious solution to still read the states is to increase the magnitude of the read bias. However, in that case, the read operation can likely affect or even destroy the encoded state, which would be highly undesirable. This issue can be avoided in cases where the length of the FEDW interconnect is well below 400 nm.

The FEDW memory cells can easily be integrated in array structures using new approaches or already well-established architectures such as cross-bar array structures (fig. S13). Future goals should be improving both the switching energy and the fatigue so as to be competitive with mature technologies such as FeRAM (35). We hope that our work will encourage rapid development toward the level of resilience demonstrated by FeRAM devices.

Nevertheless, these results provide a way forward to harness the special electronic properties of the functional FEDWs toward data storage devices. Key features of the FEDW data storage electronic devices include (i) repeated controlled creation and annihilation of reconfigurable FEDWs, (ii) large tunability of DW-controlled electrical conductivity or resistance state (OFF-ON ratio, $\sim 10^3$) of the device, (iii) low-energy operation as the information is encoded at moderate biases using specially designed geometry of electrodes, (iv) nonvolatile nature of the stored information, (v) nondestructive readout of the encoded states, (vi) high scalability, and finally, (vii) memristive functionality and large data storage densities via a precise nanoscale control of the FEDW length. In addition, the tunable memristive functionality can also be achieved by sequential injection or annihilation of an increasing number of FEDWs at precise spatial locations (23). Furthermore, this study makes a critical step toward realization of three-terminal devices such as FEDW transistor, in which a FEDW interconnect between source and drain can be electrically gated using a third terminal.

The quite diverse and wide range of ferroelectric materials includes organic ferroelectrics, which are amenable to inexpensive large-scale production by solution and spin-casting methods. Therefore, FEDW memory devices based on organic ferroelectrics offer a potential low-cost solution for mass production and their integration with flexible substrates. As a final note, FEDWs host a plethora of intriguing physical phenomena, which, among others, include magnetism in multiferroic systems (17). The magnetism at FEDWs along with demonstrated reversible creation and erasure of FEDWs in this study could potentially spur rapid progress toward the development of electrically tunable nanopintronic devices.

MATERIALS AND METHODS

Sample fabrication details

Epitaxial films of BFO were grown by pulsed laser deposition on (110)-oriented STO single-crystal substrates. A KrF excimer laser (wavelength $\lambda = 248$ nm; repetition rate, 10 Hz; fluence, ~ 1 J/cm²)

was used to ablate a ceramic BFO target with a nominal 10% excess of Bi. The substrate temperature during growth was fixed to 590°C, and the oxygen pressure was maintained at 100 mtorr. These conditions yielded typical growth rates of $\sim 0.4 \text{ \AA/s}$. After growth, the films were cooled to room temperature at 20 K/min in 5 torr of oxygen.

E-beam lithography and patterning

The devices were prepared by e-beam nanolithography, followed by physical vapor deposition of the metal electrodes. Polymethyl methacrylate (PMMA) (MicroChem) as the positive resist was first deposited on the BFO thin-film surface by spin coating at 7500 rpm for 30 s. The resist-coated BFO film was then prebaked at 180°C for 1 min before e-beam exposure. The e-beam lithography was conducted using FEI Sirion Scanning Electron Microscope (FEI) and Nanometer Pattern Generation System e-beam lithography system. The beam energy was 30 keV, and the beam current was approximately 25.7 pA for the e-beam lithography process. Both the center-to-center distance and the line spacing were set as 5.05 nm for the e-beam writing. After exposure, the films were developed in methyl isobutyl ketone/isopropanol (IPA) 1:3 for 30 s, followed by cleaning in IPA for 30 s. The device electrode was then deposited using a Lesker PVD75 e-beam evaporator (Kurt J. Lesker Company). A 3-nm Ti layer and a 12-nm Pt layer were deposited successively, both under vacuum condition below 5×10^{-6} torr. The deposition rate was 0.2 nm/s. After deposition, the film was put in *N*-methyl-2-pyrrolidone solvent and kept at 80°C for 15 min to lift off the remaining PMMA resist, leaving only the desired device patterns on the film.

X-ray diffraction characterization

X-ray diffraction was performed using a PANalytical X'Pert Pro diffractometer using Cu $K_{\alpha-1}$ radiation. For reciprocal space mapping, a 1D charge-coupled device detector (PIXcel) was used. For x-ray reflectometry measurements, a Bruker D8 Discover system was used.

SPM measurements

The SPM measurements were performed using a commercial AFM system (AIST-NT Smart SPM 1000) at room temperature under ambient conditions. Ti-Pt coated (force constant, $k = 8$ to 40 N/m) and diamond-coated ($k = 28$ to 91 N/m) Si cantilevers were used for the SPM measurements. The PFM (nonresonant PFM mode) measurements were performed using an ac imaging voltage with frequencies in the range of 600 to 800 kHz for the VPFM and 1400 to 1600 kHz for the LPFM imaging modes. The PFM response was acquired with amplitude of ac excitation set to 1.0 V (peak-to-peak) for both the VPFM and LPFM imaging modes. The electrical measurements such as spectroscopic transport measurements and 2D current maps were acquired in the c-AFM mode. In c-AFM mode, the bias was supplied to the c-AFM tip, whereas the e-beam-fabricated large Pt electrode was grounded. In our c-AFM setup, currents in the range of about 0.1 pA to 1 nA can be measured accurately.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at <http://advances.sciencemag.org/cgi/content/full/3/6/e1700512/DC1>

Supplementary Text

fig. S1. X-ray characterization of a BFO/STO (110) film.

fig. S2. E-beam lithography and metal deposition procedure.

fig. S3. DW device.

fig. S4. BFO/STO (110) coplanar switching kinetics.

fig. S5. Vector PFM of the switched domain.

fig. S6. A schematic of the ferroelectric switching process (top view).

fig. S7. Electrical poling of the BFO/LSMO/STO (110).

fig. S8. Numerical simulation of the switched ferroelastic domain.

fig. S9. Triangular or the arrow-like shape of the switched domain.

fig. S10. Switching via electric field oriented 45° to the in-plane polarization direction.

fig. S11. Sub-100-nm FEDW memory device.

fig. S12. Potential and electric field distribution.

fig. S13. Integration of FEDW memory cell in an array structure.

References (36–38)

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